Close

Ultrathin, stackable QFN packages

EXECUTIVE OVERVIEW

Three-dimensional packaging generally has at least two significant goals: the achievement of higher conduction speed and the reduction in overall volume of component packages. One of the earliest and most innovative efforts is the chip-in-polymer program at Fraunhofer IZM in Berlin -- a concept patented by Fraunhofer in 1999. This program achieves 3-D advantages by embedding the chip in a polymer. A chip embedded in polymer has excellent protection from shock and vibration, and lends itself to shorter interconnect distances that can enhance performance. This article describes the advances to date with this technology.

December 7, 2009 - Typically, the chip-in-polymer process starts with a thinned chip that is adhesively bonded to a thin substrate, then overlaid with resin-coated copper (RCC), consisting of a resin layer ~80µm thick with a 5µm copper surface. When the resin has cured, vias are laser-drilled by a 335nm ultraviolet (UV) laser down to the contact pads on the chip. The vias are plated with metal, and the redistribution layer on top is etched from the copper.

Fraunhofer IZM typically adds one twist to its development projects: it aims to design packages that can be used in commercial production without specialized equipment or other delays. Its most recent project, which is nearing commercial viability, is a polymer-embedded QFN, so called because it is essentially a quad pack with no leads, the leads being replaced by pads on the bottom surface. The QFN is being developed as part of the HERMES project that comprises Fraunhofer and ten other European industrial or academic partners in the advancement of chip embedding technology.

The QFN was selected for development because QFNs are commonly used as micro-controllers in small, thin appliances. Because QFNs have no leads, they do not require a lead frame or connection to a lead frame. Team leader Andreas Ostmann points out that the target of development could have been a BGA, but the overall thickness of whatever embedded design was achieved would have been compromised by the thickness of the balls. QFNs can be connected directly to a flat solder layer on the board. Another benefit of the QFN choice for an embedded package: the embedded QFN is easy to test electrically before it is shipped to a customer, or, in Fraunhofer's case, subjected to other tests. Ostmann also thinks that the large number of component package types currently being used will shrink, perhaps dramatically, and that QFNs will take over many application niches currently held by other types.

The embedded QFN developed by Fraunhofer contains a chip measuring 5mm × 5mm and thinned to 50µm; the package itself measures 10mm × 100mm. The 84 I/Os on the chip are at 100µm pitch, and on the package at 400µm. At the moment, the QFN is made by conventional substrate structuring and had 50µm line widths, but Ostmann plans to move to a semi-additive process that will permit line widths and space widths of 20µm. One problem that came up during development was that the lines and capture pads lay on top of the vias that were also 50µm wide. Etching of the copper layer to create the lines and spaces inevitable etched away the sides of the vias as well. The solution was to increase tolerance by reducing the via diameter to 30µm (**Figure 1**).

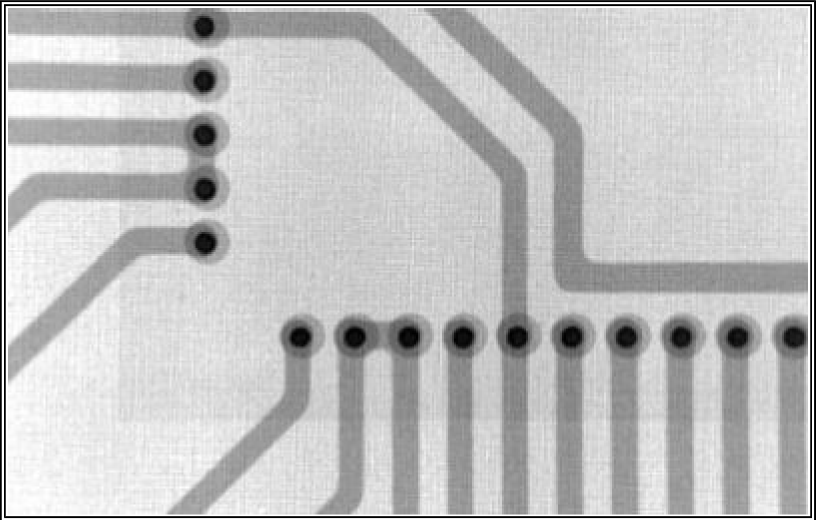

Figure 1. An X-ray of lines and vias shows the results of reducing via diameter to 30µm.

The chip is adhesively bonded to an FR4 core that is also 50µm thick. When the chip is overlaid with resin and copper, the final package is 160µm thick. Later this year, Ostmann says, the 50µm thick FR4 core may be replaced with a much thinner copper core. This change would bring the overall package thickness down to 110µm. One of the reasons for the minuscule z-dimension is to permit stacking of the QFNs without putting constraints on the design of the appliance. A theoretical stack of ten 110µm QFNs, for example, would have a thickness of only slightly more than 1mm.

The current 160µm QFN caused a few surprises when the first samples were imaged acoustically at Sonoscan's applications laboratory outside Chicago. The laboratory has seen plenty of QFNs, but always with much larger vertical dimensions. The technician imaging the Fraunhofer packages on a Sonoscan C-SAM system noticed immediately that the whole package is roughly as thick as a single depth of interest might be on another package. The distance from the distribution layer at the top surface to the die surface is only ~60µm. The dimensions made it possible to image the QFN package with an ultrahigh frequency, high-resolution 230MHz ultrasonic transducer.

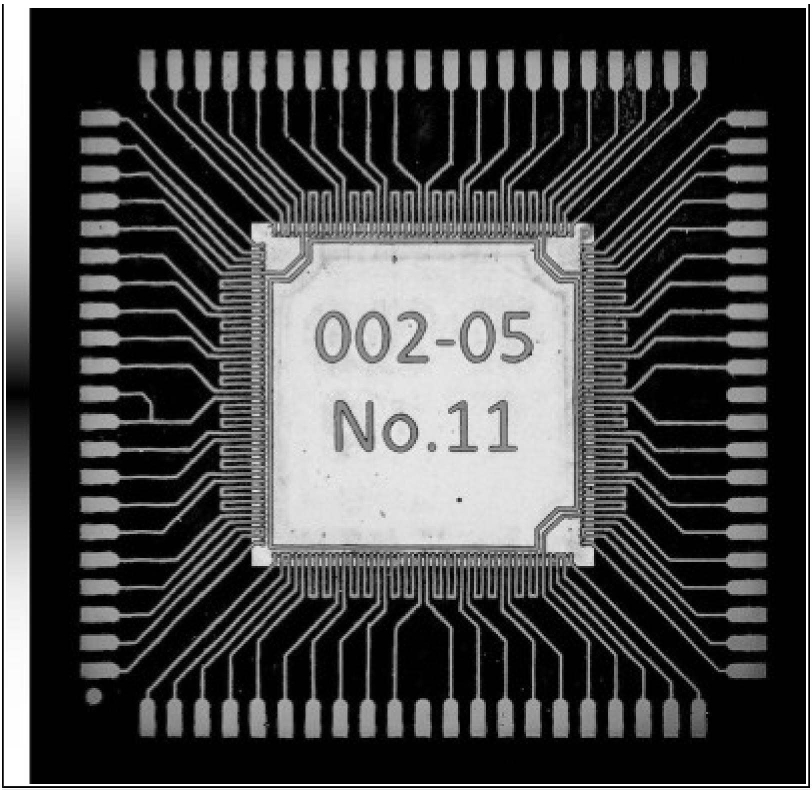

Figure 2. 230MHz acoustic image of die-to-polymer interface shows absence of anomalies or defects at this critical depth. Package thinness permits higher acoustic frequencies with higher resolution.

The die surface (**Figure 2**) is always of interest acoustically because of the delaminations or other potentially lethal defects that may lurk there. One immediate observation: acoustic access to this interface is made easier by the thinness of the package. The acoustic image in Fig. 2 shows a complete lack of anomalies at this interface. Another interface of interest, for similar reasons, is the bond of the die to its substrate. This interface was also free from problems. The only anomaly seen acoustically was a less reflective, darker area (**Figure 3**) in a scan gated just below the redistribution layer at the top of the package. This anomaly probably represents some localized material change in the cured resin beneath the redistribution layer, and is not likely to be significant for performance or reliability.

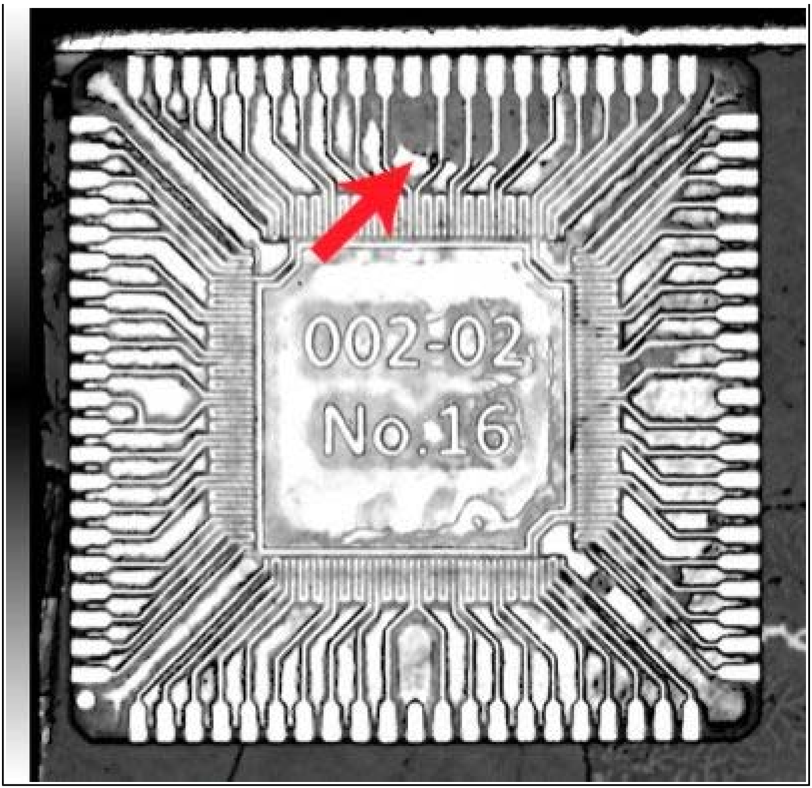

Figure 3. Acoustically darker region (arrow) in polymer probably represents a harmless local material variation.

Lab personnel imaging the QFNs noted that their thinness and good acoustic qualities would make them easy to image at high resolution even after surface-mounting, something that is not always true of conventional packages. The same would probably be true if the QFNs were packaged in the alternate configuration that the Fraunhofer team has planned, with the die face down and the vias extending to the back side of the package.

Acoustic micro imaging was also used in a different technique to check the acoustic surface flatness (ASF) of the QFN package. During standard imaging at any selected depth, a portion of the pulsed ultrasound is reflected from the top surface of the part. The separate ASF module (Sonoscan patent pending) measures the round-trip travel time (but not the amplitude, polarity, or other characteristics) of the ultrasound reflected from the top surface. This data is used to assemble a topographic map showing the surface flatness of the part. The acoustic surface flatness image of one of the QFN packages (**Figure 4**) shows that there is some variation in flatness, but no gross deviation. X- and Y-axis measurements are in tenths of an inch. The greatly exaggerated Z-axis measurements are in thousandths of an inch.

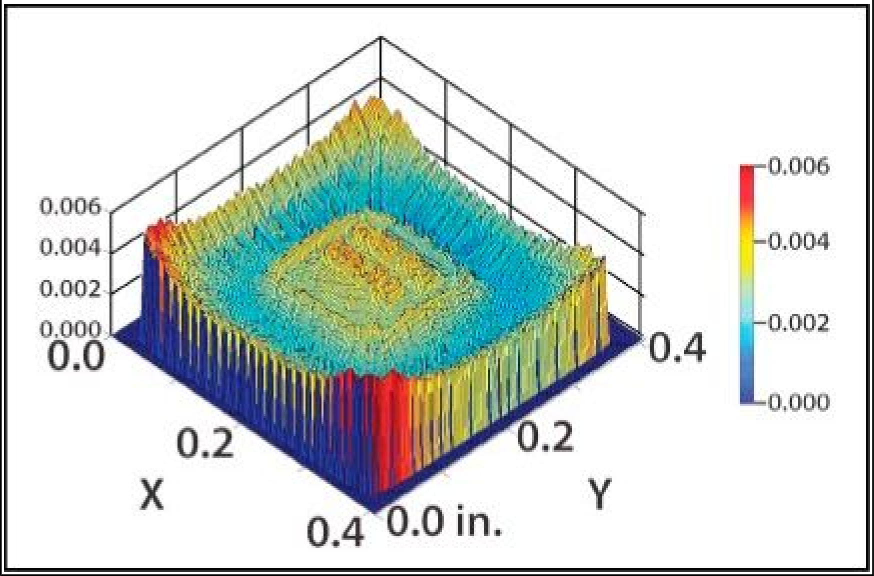

Figure 4. Acoustic surface flatness (ASF) image, made by measuring the round trip time of thousands of pulses, greatly exaggerates the z axis, but shows only slight variation across the surface of the package.

The QFN package recently passed moisture sensitivity testing (168 hours at 85°C and 85% relative humidity, followed by reflow at 260°C) without incurring defects such as delaminations. Ostmann estimates that commercial production of QFNs with 120µm pads and 150µm pitch can begin in 2010, and finer geometries such as 100µm pads, in 2011. The overall design will lend improved electrical performance and improved reliability to anticipated applications such as household power modules, communication modems, motor control units and secure phone modules.

ACKNOWLEDGMENTS

C-SAM is a registered trademark of Sonoscan.

BIOGRAPHY

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