Thermal Impedance Monitoring during Power Cycling Tests

Alexander Hensler, Chemnitz University of Technology, Germany
Christian Herold, Chemnitz University of Technology, Germany
Josef Lutz, Chemnitz University of Technology, Germany
Markus Thoben, Infineon Technologies AG, Germany

Abstract

In this publication a new method of thermal impedance analysis of power modules is presented. It enables a distinction of different failure mechanisms within the heat flow path by electrical measurement during power cycling tests. With measurement and evaluation of the thermal impedance $Z_{th}$ the degradation can be located within chip solder layer, system solder layer and thermal interface material.

1 Motivation

Reliability of power modules at power and thermal cycling load is determined by the deterioration of the heat flow path between die and heat sink or coolant. Up today during accelerated reliability tests this failure is detected by increase of the online measured quasi steady-state thermal resistance $R_{th}$. Thereby the increased $R_{th}$ is caused by degradations in different layers of the heat flow path of the module between junction and reference temperature point, usually the case or heat sink temperature. By standard the failure criterion is a 20% increase of the initial value. The monitored trend of the $R_{th}$ does not provide any information which layer degraded. Further, due to noisy measurement data, low variations of the thermal resistance caused by the deterioration of materials remain undetected. Therefore the failure analyses are performed subsequently with Scanning Acoustic Microscopy, X-ray or metallographic preparation to obtain more detailed information about the aging status of the power module. These analyses are time-consuming, several of them destructive and do not always deliver convincing analysis results.

The monitoring of thermal impedance parameters promises a simpler and faster non-destructive analysis method for power modules during reliability tests.

2 Thermal Simulation

First, the transient thermal behaviour of a typical power module with a base plate was simulated using equivalent CAUER-Network. The aim of this simplified model was to reproduce the effect of the failure within a specific material layer on the $Z_{th}(t)$ function. The basis of the simulation is a power module mounted on a liquid-cooled copper heat sink as depicted in Figure 1.

![Figure 1: Basis of $Z_{th}$ simulation, power module mounted on a liquid-cooled copper heat sink](image)

Each layer of the heat flow path was simulated by two thermal resistances and one thermal capacity. Thereby the thermal spreading was simplified and considered an angle of 45°. The heat flow area increases accordingly along the heat flow path from chip towards coolant. The equivalent circuit of one
single material layer is depicted in Figure 2 (left), the total thermal system is depicted in Figure 2 (right).

![Thermal Circuit Diagram](image)

**Figure 2**: CAUER based thermal circuit for simulation of different failures

Values of thermal resistances and capacitances of the whole thermal system were calculated with the typical power module data presented in [1]. The chip area was about 2 cm². The temperature dependency of material properties was neglected. The thermal impedance is calculated between the chip and the coolant accordingly following equation (1). The coolant temperature is assumed constant and represents the reference point $T_{\text{ref}}$.

$$Z_{\text{th}} = \frac{T_j - T_{\text{ref}}}{P_V}$$

(1)

With the simplified simulation model three typical failures were investigated: degradations of chip solder layer, system solder layer and thermal grease (TIM). For each type of failure the area of the corresponding layer was reduced in order to increase the whole thermal resistance between junction and coolant by 20%. The result of this simulation is shown in Figure 3. This result shows that different failures lead to different $Z_{\text{th}}$ curves. Different time points for the splitting of the curve with failure from the curve without failure can be distinguished. In [2] this effect was used experimentally to observe chip solder layer degradation of high power modules during power cycling tests. $Z_{\text{th}}$ values were measured at two different time points. Thereby the chip solder layer failure could be distinguished from the thermal grease effect. The separation of the system solder layer failure from the chip solder layer was not possible with this method.

![Simulated Z_th Curves](image)

**Figure 3**: Simulated $Z_{\text{th}}$ curves of different failures

The $Z_{\text{th}}(t)$ function is usually described using equations (2) and (3), which represent the equivalent FOSTER-network (Figure 4 left).

$$Z_{\text{th}}(t) = \sum_{i=1}^{n} R_i \left( 1 - e^{-\frac{t}{\tau_i}} \right)$$

(2)

$$\tau_i = R_i \cdot C_i$$

(3)

In data sheets for the $Z_{\text{th}}(t)$ function mainly four or five RC elements are used. It is sufficient for an acceptable approximation of a real measured thermal transient curve. The equivalent FOSTER-circuit can be used for the proper calculation of the whole given thermal system. The nodes between RC elements of this circuit do not refer to specific geometric points of the thermal system [3]. Therefore with this network a physical interpretation of partial thermal areas within the heat flow path is not possible. The correct physical description of partial thermal resistances gives the equivalent CAUER network as seen in Figure 4 (right). However, this circuit cannot be extracted directly from the measured $Z_{\text{th}}(t)$
function, since many solutions are possible. In order to obtain a CAUER-network, first, the equivalent FOSTER-network has to be extracted from the \( Z_m(t) \) curve. After this, with the network transformation the equivalent CAUER network can be calculated. At that the number of RC elements is equal in both equivalent circuits.

![Figure 4: Equivalent networks for description of thermal systems](image)

The approach for the localisation of different failures within the heat flow path of a power module is the monitoring of CAUER \( r_i \) parameters. The schedule of this method is as follows:

- Measurement of the \( Z_m(t) \) function
- Extraction of the equivalent FOSTER network with an approximation method (e.g. [4])
- Transformation of FOSTER into CAUER equivalent circuit (e.g. [3])
- Monitoring of CAUER \( r_i \) parameters

First, this method was verified with the simulation data. With the method of [4] the \( Z_m(t) \) curves from Figure 3 were approximated with the equation (2). With eight elements the best fit could be reached. After the approximation the FOSTER-network was transformed into the CAUER-network. For this transformation the method of the recursively rapid FOSTER-CAUER circuit transformation was applied described in [3]. The partial CAUER thermal resistances of simulated failures are compared in Figure 5. Obviously, for a specific failure only one partial thermal resistance has a significant increase in comparison to the \( r_i \) values without degradation. Other elements remain nearly unchanged. These points are marked with arrows.

![Figure 5: Partial thermal resistances of CAUER circuit, results of simulated failures](image)

A \( r_i \) element cannot be referred to a certain material layer, since the number of extracted RC elements does not correspond to the number of layers. However, CAUER elements indicate specific physical area within the heat flow path. Thereby the \( r_i \) order relates to the direction from chip to coolant. The correlation of \( r_i \) to a specific part of the heat flow path can be estimated by comparison between extracted CAUER \( r_i \) and \( C_i \) values and values of the known real power module package.

In summary, it can be stated that the monitoring of CAUER-parameters can be a possible method for the separation of different failures.
3 Experimental Results

The monitoring of CAUER $r_i$ parameters was investigated experimentally with a superimposed power cycling test. The device under test was a standard power module of the manufacturer Infineon Technologies AG as shown in Figure 6.

For the test the power module was mounted on a liquid-cooled copper heat sink. With an external heating/cooling station the power module was heated and cooled passively. During heating phase power cycles were superimposed. Test parameters are shown in Figure 7. The maximum junction temperature and maximum case temperature are beyond the specifications of this power module type.

![Figure 6: DUT (standard power module), Test set-up](image)

![Figure 7: Test parameter of superimposed power cycling test](image)

During the test the thermal impedance was measured periodically every 20 passive cycles. For this measurement the cycling test was interrupted at the lowest coolant temperature at the end of the cooling phase. After that a load pulse was applied with 250A load current, 30s heating and 30s cooling time. The $Z_{th}(t)$ was measured between junction and case during the cooling phase. The junction temperature was measured with the $V_{CE}(T)$-method described in detail in [5]. The case temperature measurement was realised with a thermocouple beneath the active chip area as shown in Figure 6 (right). The power losses of the IGBT were measured at the end of the heating phase. The $Z_{th}(t)$ was determined according equation (1). After that, the equivalent FOSTER circuit was approximated with the least square fit method. The best fit corresponding to the equation (2) could be reached with four RC elements. In comparison to simulation result less elements were sufficient.

The measured thermal impedance $Z_{th}(t)$ of IGBT 21 and the result of the mathematical approximation are shown in Figure 8.

Finally, the CAUER elements were calculated with the circuit transformation algorithm from [3]. The partial CAUER $r_i$ elements were monitored during the test. The trends of these parameters are seen in Figure 9.
DUTs show in Figure 9 different deterioration behaviour. IGBT 21 shows a significant increase of the $r_2$ parameter whereas this parameter of IGBT 22 remains constant. A reverse behaviour is seen in the parameter $r_1$. The relation of $r_i$ to a certain layer of the heat flow path is based on time constants of RC elements. The partial $r_i$ parameters split the power module package in parts corresponding to $\tau_i$ and $r_i$ values of RC elements. Determined CAUER parameters of IGBT 21 are listed in Table 1. Based on typical packaging parameters from [6] the heat flow path regions were estimated and referred to the measured CAUER elements, seen in Table 1.

<table>
<thead>
<tr>
<th>Order</th>
<th>$R_i$ [K/W]</th>
<th>$\tau_i$ [s]</th>
<th>Heat flow path region</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>70.5m</td>
<td>24.4m</td>
<td>Chip – Al2O3 base plate</td>
</tr>
<tr>
<td>2</td>
<td>52.4m</td>
<td>88.7m</td>
<td>Al2O3 – TIM base plate</td>
</tr>
<tr>
<td>3</td>
<td>38.3m</td>
<td>711m</td>
<td>Base plate – TIM</td>
</tr>
<tr>
<td>4</td>
<td>10.6m</td>
<td>4.44</td>
<td>TIM – heat sink top side</td>
</tr>
</tbody>
</table>

Table 1: Measured CAUER parameters of IGBT 21 (test start)

Corresponding to this estimation of the certain heat flow path regions the trend of CAUER parameters in Figure 9 show that IGBT 21 should have a significant degradation within the system solder layer and IGBT 22 degradation within the chip solder layer. Furthermore the effect of the TIM (thermal grease) in the trend of $r_3$ and $r_4$ is displayed.

The failures were confirmed with Scanning Acoustic Microscopy as shown in Figure 10. In the right image the delamination of the system solder layer is seen clearly as bright regions beneath IGBT 21.
IGBT 22 shows no degradation in this layer. It is conform to the trends of the electrically measured CAUER parameter $r_2$ in Figure 9.

In regions of the IGBT chips the inhomogeneity of the left image can be interpreted as a beginning degradation. Electrical measurements in Figure 9 (parameter $r_1$) emphasize that IGBT 22 must have a higher degradation than IGBT 21 in the chip solder layer.

![Figure 10: Analysis with Scanning Acoustic Microscopy (view from the base plate)](image)

left: chip solder layer, right: system solder layer

4 Conclusion

The monitoring of CAUER partial thermal resistances is a suitable method for the online analysis of power modules during power cycling tests. Failures within the heat flow path could be detected precisely, although the conventional method of the $R_{th}$ (junction – case or coolant) monitoring showed no significant increase. The calculation algorithm requires only moderate computing effort. So it can be implemented in the control software of the power cycling test.

Moreover, the analysis of the transient thermal behaviour offers a potential for a fine resolution analysis of the heat flow path, which is the target for further investigations.

5 Acknowledgement

The authors would like to thank Daniel Wingert (TU Chemnitz) and Mark Tüllmann (Infineon Technologies AG) for contribution to this paper. The work was supported by grants of the German Federal Ministry of Economics and Technology (BMWi).

References