Advanced Packaging

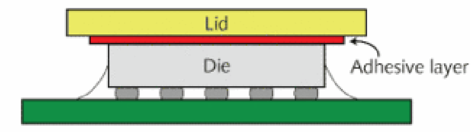

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Figure 1. *Side view showing device structure.*

Nondestructive Bondline Measurement in Advanced Flip Chips

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A key feature of high-performance flip chips is their thermal budget. Because of their high current load, these die, usually large in area and often used as microprocessors, need an efficient and reliable method of heat dissipation.

A standard method is to attach a metal lid to the backside of the flip chip (**Figure 1**). Various materials have been used to join the lid to the chip. One example is a resin-based, silver-filled adhesive having high thermal conductivity. It differs from somewhat similar adhesives used in die attach because its viscosity is 3– 4 times higher. Mounting the lid onto the flip chip backside is a critical process step. The thickness of the adhesive is especially critical industry-wide; the desired thickness of the adhesive in these applications generally ranges from 50– 100 µm.

The relationship between the adhesive thickness and thermal conductivity is complex. In theory, to achieve the highest thermal conductivity, the bondline of the adhesive should be as thin as possible. Mechanically, however, thin bondlines do not work well because delaminations tend to form along them over time, functioning as insulators that obstruct thermal flow from the chip. A bondline thickness ranging from 20– 30 µm would be expected to delaminate at some point after assembly. The thickness at which delaminations are likely to form varies with the size of silver particles in the resin, and is the result of thermal mismatch between the adhesive layer and either the die or lid.

Overheating of the chip can also occur if the adhesive bondline becomes too thick. For example, if the thickness of the adhesive layer increases from the specific thickness of 75 µm to 100 µm, the temperature of the chip is likely to increase by 0.5°C– 1.0°C/watt (W) of input. If the input wattage is, for example, 50 W, and the bondline thickness causes an increase of 0.5°C/W, the temperature increase will be 25°C. Since the actual operating temperature of the chip is over 100°C, even an increase of 0.5°C/W becomes critical for high power applications.

One method of bondline thickness measurement* uses an automated acoustic micro-imaging system that handles parts in JEDEC-style trays. This nondestructive alternative to destructive physical analysis (DPA) was developed to permit measurement of the adhesive bondline as soon as possible after joining the lid with the backside of the flip chip. The purpose of acoustic measurement is to identify process trends — such as a condition where bondline thickness is drifting higher — rather than identify individual chips as rejects. Automated acoustic measurement avoids the necessity of sending parts to a laboratory for potting, sectioning, and polishing to measure the thickness. Aside from the inevitable loss of good parts, accurate and thorough DPA physical sectioning takes anywhere from one to two days, during which time a great number of defective parts might be produced. Automated acoustic measurement gives almost real-time feedback that keeps the number of defective parts at a minimum, enhancing overall yield.

Most acoustic micro-imaging involves the production of acoustic images, but in this application, only data referring to the thickness of the bondline is needed. Acoustic micro-imaging systems, whether making images or providing data, detect the time that an ultrasonic pulse requires to travel through a material layer having a known acoustic velocity. The transit time, polarity, and amplitude of return echoes can be visualized in a waveform (**Figure 2**). When the travel time and the acoustic velocity of the material are known, the thickness of the material is easily calculated. In a multilayer sample, waveforms display interfaces between various materials. The acoustic waveform of a plastic-packaged IC such as a PQFP, for example, will display a waveform peak at the interface between the plastic and the silicon die, and a second waveform peak at the interface between the silicon die and the die-attach material.

In the devices discussed here, the three materials involved are, in order from the top surface, the metal lid, adhesive bondline, and silicon chip. The two interfaces of interest are lid-to-adhesive, and adhesive-to-chip. Although the adhesive bondline is itself thin (80 µm), the overall assembly is fairly thick, and lower rather than higher acoustic frequencies are used. A key problem that needed solving during development was the proximity of key echoes to each other. Because the adhesive is so thin, the two ultrasonic echoes from each side of the adhesive bondline arrive at the transducer at nearly the same time, and the echoes begin to merge. Software that attempts to use these two echoes alone to measure bondline thickness tends to lose the second echo because it is so close to the first echo. But without the second echo, thickness cannot be measured.

A solution to this problem was found. The flat metal lid is larger in area than the chip itself, and air is beneath the outer area of the lid, rather than the adhesive. The echo that is returned from the interface between the lid and underlying air has high amplitude and is not, at its location away from the adhesive, near another interface. To determine the thickness of the adhesive, the echo from the lid-to-air interface was used in place of the lid-to-adhesive interface, while the echo from the adhesive-to-chip interface was used as the second echo. The travel time between these two echoes could then be used to accurately determine the bondline thickness. The fact that one echo was "borrowed" from a nearby location had little impact on accuracy because the materials involved are homogeneous and flat. (To handle situations where the area of the lid is not larger than the area of the chip, software exists that separates the two echoes, so that a reference echo is not required.)

In production, JEDEC-style trays of parts are fed into the automated acoustic micro-imaging system shortly after the lid has been attached onto the back of the chip. The imaging system's transducer makes a thickness measurement at nine locations. Each of these thickness values, along with the average thickness for the chip and the minimum and maximum values, are used to determine accept/reject status. Early detection of thickness values that have begun to drift outside of the required parameters makes it possible to alter processes at a point when few rejects have been assembled. When the line is restarted after process modification, the new thickness values can also be obtained quickly.

** developed by Sonoscan in conjunction with Texas Instruments.*

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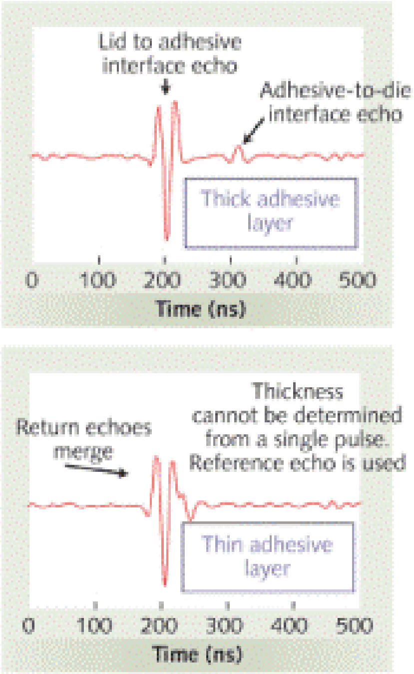

Figure 2. *Thickness of a relatively thick layer (top) can be measured because the two return echoes are widely spaced, but very thin layers (bottom) require a different method.*

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