Flip chips: Simultaneous multi-gate acoustic imaging

Finding structural defects and anomalies in a flip chip assembly means having a clear and nondestructive view of the interior. The design of flip chips gives a substantial advantage to acoustic micro imaging tools: with current ultrasound technology, silicon is an excellent medium through which sound travels with minimal detectable defects.

This transparency means that ultrasonic transducers pulsing ultrasound at high frequencies can be used to provide high resolution in the acoustic images. High resolution is needed to evaluate the degree of risk of a particular anomaly.

High-frequency transducers, however, provide high resolution only in the x and y axes. To make an acoustic image of any sample, the returning echoes are typically gated on a depth of interest. The arrival time of an echo is used to verify that the feature from which the echo was returned lies within the depth of interest - the gate. Echoes from features beyond the gate are ignored, while defects before the gate will cast shadows below.

In imaging flip chips, there are likely to be features of interest at any depth between the chip face and the substrate. Gating on the whole depth of the underfill may image all of these features, but it may be difficult to determine the relative depth of a particular feature. Because the air within the void does not transmit ultrasound, the bottom side of the void is not detected unless the bottom side of the sample is scanned. If there are multiple features of interest it makes sense to use a narrower gate.

To gather more comprehensive depth data, Sonoscan has developed a method that collects echoes from multiple gates during a single transducer scan. The image of a flip chip typically is made up of millions of pixels, each pixel representing the amplitude of the echo from one of the x-y locations into which a pulse was sent. Gap-type features return the strongest echoes - essentially 100% of the pulsed ultrasound. Bonded interfaces return moderate-strength echoes, and locations with no features return no echoes.

The new method permits the system operator to enter the number of gates desired, as well as the position and width of each gate. The gates may all have the same width, or different widths. They may be adjacent to each other, separated, or overlapping. In any of these configurations, software uses the echoes collected from each gate, and then produces a separate acoustic image. The scan time for the flip chip, however, is not increased by using this method.

How this method was used is shown in Figure 1: six gates were set, of equal width, extending from the back of the chip to the top of the substrate. Adjacent gates overlap slightly to ensure complete coverage in the vertical dimension. In other words, the underfill region of the flip chip was sliced horizontally into six equally thick, slightly overlapping layers in order to produce an acoustic image of each layer.

Figure 2 is the acoustic image of gate #1, just below the chip face. This flip chip measured 14.9 x 11.0 x 0.8mm. The faint horizontal and vertical lines are the result of the traces on the chip face being just within the gate. It is immediately evident why this chip was selected for discussion: the number and variety of defects. Red identifies highly reflecting features that are within gate one.

The large irregular red features, mostly in the top half of the image, are regions of more highly concentrated filler particles caused by the non-homogeneous nature of the underfill. In some instances the tip of a particle group contains a tiny void. When fluid underfill locally has too many filler...
particles and too little resin, voids are likely to form. A larger void, also associated with particle clumping, is marked by a yellow arrow. The void itself appears grey because the peak of the void lies just below gate #1. Two additional grey voids are located near the bottom centre of the chip. During scanning, ultrasound is reflected from all depths. Ultrasound reflected from lower interfaces in the assembly is blocked by these voids, which therefore appear in gate #1 as dark acoustic shadows.

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Near the bottom right corner of the flip chip is a dark edge feature, outside of gate #1 and possibly a surface feature, chipout or crack. To its left, along the bottom edge of the chip, are four edge voids. There are two similar voids along the top edge of the chip.

Figure 3 shows an area in gate #1 just to the right of the grey void. This area contains a resin-starved particle clump (arrow) that may be a danger to long-term reliability. The clump appears to be parallel and in contact with the long vertical row of solder bumps. Closer inspection shows that it has surrounded a shorter vertical row of three bumps and is in contact with the longer row of bumps as well. Failure can occur when the solder flows into the spaces between the clumps until the solder bump collapses and breaks its connection. At the top centre of Figure 3 a particle clump has deposited excess particles in the vicinity of solder bumps, although the density of the particles is less.

Figure 4 is the acoustic image made at gate #2, the second of the six gates. Comparison to gate #1 shows that:
- Both gates catch a portion of the echo. The pulse of one echo is wide enough to be found in both slightly overlapping gates.
- The large circular void marked by an arrow in Figure 2 is red in this image, rather than grey. The top surface of the void clearly lies within gate #2. The same is true of the two additional voids near the bottom centre of the chip.

These two grey-outlined voids are shown in greater detail in Figure 5, which shows that there are two smaller grey-ringed voids in the groups of solder bumps at bottom, for a total of four voids. Unlike the other voids in the underfill of this flip chip, these four voids are not associated with particle clumps, but are probably the result of anomalies in the flow of the fluid epoxy. All four voids are in contact with solder bumps, and thus pose a risk to future reliability.

The data from gate #3 is shown in Figure 5. The particle clumps have lost the red colour indicating high amplitude reflection, indicating that the chip to dense particle interface lies above this gate. The three largest voids or void areas are still red, however. The edge feature near the lower right corner displays, at this depth, a tiny red area characteristic of a gap, which in this case may be a void.

Figure 5: Details of voids in contact with bumps in gate 2.

Figure 6: Voids extend into gate 3, but particle concentrations do not.