



Removing Hidden Internal Packaging Defects From Production

By Tom Adams

Integrated circuits often fail, not because of some defect in the circuitry of the chip, but because of a defect in the attachment and encapsulation around the chip. Packaging of the chip is one of the last steps in production, and is usually followed by mounting of the finished component onto a board, tape, or other structure.

Nearly all hidden internal defects in plastic IC packages either occur at interfaces between layers of material (a delamination between the chip face and the plastic of the package, for example) or involve the creation of a new interface (a void in the die attach holding the chip to its substrate). A few defects involve no gap-type defect such as a delamination or a void, but consist of an internal feature which is out of place. A die tilted out of horizontal is one example.

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Hidden internal defects may eventually “kill” the chip by creating some kind of break in the circuitry. Most often, a defect breaks an interconnect such as a lead wire or a solder bump. Sometimes the defect actually cracks the die (disrupting the circuitry on the face of the die) or, by causing the die to overheat, burns up circuitry on the die.

This damage occurs when the hidden defect has expanded beyond its original size. The expansion is often caused by the repeated heating and cooling that computers and other systems regularly go through as they are turned on and off, but can also be caused by environmental contaminants or mechanical shock. For example, a delamination — by definition simply a gap between two materials where no bonding has occurred — usually grows not by expanding the disbond but by radiating horizontal cracks.

No Damage, Yet

The danger posed by hidden internal defects is especially great because many of them, in their original form, have not yet caused any damage, or, more significantly, any electrical symptoms. Manufacturers routinely perform electrical tests on packaged ICs, and packages having internal defects regularly pass these tests. Manufacturers also regularly x-ray parts, but nearly all hidden internal defects are much too thin to show up in an x-ray image.

As a nondestructive method for imaging internal features, x-ray is nearly a century old. A much newer method, acoustic micro imaging, uses very high frequency ultrasound, and has the advantage of being sensitive to internal interfaces between materials, and especially to internal gap-type defects such as delaminations, voids, cracks, and disbonds. If you pulse very high frequency ultrasound into a part, each well-bonded interface will bounce back part of the signal; this reflection permits well-bonded features to be imaged. Gap-type internal defects, though, will bounce back all of the ultrasound, and are imaged with even greater intensity.

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Many failure analysis laboratories use acoustic micro imaging systems to both image and analyze hidden internal defects nondestructively in packaging operations. Ultrasound, generally ranging from 10MHz up into the hundreds of MHz, is pulsed into the IC package to create a visible acoustic image. A flip chip package might show a delamination (a highly reflective gap-type defect) between the chip face and the epoxy underfill material. The location of the delamination may give clues to its cause — contamination of the die face and improper heating during underfill are two possibilities. The failure analyst is helped in his analysis by the fact that the return echoes from inside the package can be gated to a specific depth; he can use only the echoes from the chip-underfill interface to make the visible acoustic image, and discard echoes from other depths within the package.

Conventional acoustic micro imaging systems are designed for laboratory use and can take only a limited part in production inspection. A failure analyst considers himself pressured if he has a dozen parts to image and analyze.

A new automated system developed by Sonoscan takes the same technology and moves it directly into the production stream, and provides throughput ranging up to several thousand parts per hour. This system positions the defect sensitivity of acoustic micro imaging exactly where it will spot hidden internal defects before the IC packages are used in assembly.

Elements in Straight Line

The system has five elements arranged in a straight line: an input elevator which holds a stack of JEDEC trays; a conveyor which brings one tray at a time to the scan area; the scan area which has a very fast-moving ultrasonic transducer; a conveyor exiting the scan area; and a restacking elevator to hold the scanned trays.

Transducers used in the system are the same as those used in Sonoscan's laboratory systems — there is no compromise in image or data quality. But the transducer in the automated system scans far more rapidly.

Return echoes can be gated on a depth of interest in the package, or even on multiple depths, with no loss of throughput speed.

As in a laboratory system, the return echoes can be gated on a depth of interest in the package, or even, with no loss of throughput speed, on multiple depths. The acoustic image of each tray of parts is stored electronically, but in normal use, these images are not often viewed. The system is automated, and no technician is needed to view the images; moreover, the work of eliminating hidden internal defects after they have been found can be accomplished by an optional pick-and-place machine. The pick-and-place moves the first tray imaged to one side and removes defective packages from it. As subsequent trays are scanned (as rapidly as 51 seconds per tray), the pick-and-place removes reject packages and replaces them with good packages from the reserve tray. All hidden internal defects are removed from the production stream.

The system will handle any part which can be imaged acoustically and which will ride in a tray. Its application has spread rapidly from IC packages (for which JEDEC trays are normally used) to many other samples, including:

- Singulated IC packages in trays.
- Bonded wafer pairs, where the usual defect is microvoiding or lack of bonding between the wafers.
- Ceramic chip capacitors.
- Packaged and unpackaged ICs in strip form.

When strips of ICs are placed on a tray, the area of interest is the package itself, not the lead frame beyond the package. To make imaging of strips even faster, a “partial scan” mode is used in which the transducer images the rows of packages but skips the non-interest areas between the rows.

Users of the system in production environments are often looking primarily for a single type of defect, and gate the depth of the return echoes accordingly. The defect of interest may be a die face delamination in a conventional package, or a

delamination between the die and underfill in a flip chip package. Accept/reject criteria are defined by the user; software routines are written by Sonoscan to match these criteria. In some applications users define three levels — accept, reject, and marginal.

The automated acoustic micro imaging system (Sonoscan calls it the FACTS2) gives manufacturers a means to identify hidden internal defects and remove parts having these defects from production. It permits manufacturers to achieve high reliability in an area where they have long been vulnerable — the hidden internal defects which pass electrical tests but later turn into field failures.

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