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Electronic Packaging

Exploring the Flip Chip to Achieve High Reliability

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Incorporating a flip chip into a product can be a viable option for medical electronics. Production processes must be developed that achieve short assembly time, low cost, and high reliability.

Advanced chip packages offer advantages such as smaller size and shorter connection distances that cannot be gained from more-conventional electronic packages. But using advanced packages in high-volume production requires careful planning of production processes to avoid costly interruptions. (See the sidebar "Key Points of the Flip Chip Package," below)

Flip chip packages position the chip face down. Bond pads on the face of the chip are connected by solder bumps to the substrate. This configuration produces a low profile and eliminates the need for wire bonds. A successful flip chip design is potentially less costly than other package types. Although flip chips can sometimes be difficult to work with, when they are properly designed and executed, they are very reliable. A flip chip package design eliminates the problems associated with solder balls being missing, bridged, cracked, or voided. In addition, the underfill material fills the entire underchip cap without defects, and the fluid underfill can be flowed into the gap quickly enough to allow high-speed production. The fluid underfill cures in a reasonably short time.

Figure 1. Panel of 63 substrates with all components in place.

This article explains the development of a flip chip process designed to integrate the chip into a product quickly and reliably. For this application, the work was carried out at the Fraunhöfer Institute (Berlin). The original equipment manufacturer (OEM) required that the flip chip process provide a short assembly time, an assembly cost less than that of a surface- mounted device (SMD), and high reliability. The flip chip used was an application-specific integrated circuit (ASIC) and was part of an electric circuit for power switching, timing, and other functions in the product. The chip measured 2.9 x 1.4 mm with 23 input/outputs (I/Os) and had a minimal pitch of 150 µm. Assembly of the flip chip onto the substrate consisted of bumping of the flip chip, flip chip placement, reflow soldering, and underfill dispensing.

Chip Bumping

The chip supplier performed the chip bumping, but subsequent processes were optimized for high-volume production at the institute. There are two primary methods of bumping flip chips. A well-established, but costlier, method uses sputtering and electroplating to put down the thin layer of underbump metallization that protects the aluminum bond pad from the solder. This method uses photolithography for solder deposition, which makes it possible to achieve very low pitches. This method was used by the supplier.

A second, less costly method lays down the underbump metallization by chemical metal deposition; this method is often called electroless nickel (Ni) bumping. The solder is then applied by stencil printing. In production, the use of stencil printing usually limits pitch to 200–250 µm, but this method can accommodate a variety of solders, including lead-free solders.

Packing Chips

The packing method chosen for shipment to the assembly house also involves cost considerations. The packing costs affect the overall cost of the chip, so it is important to select the most cost-effective method. In this case, the supplier delivered the chips in waffle packs. Most placement machines can handle waffle packs, but the cost of shipping includes the empty packs. Alternatives include tape and reel (which, like waffle packs, includes higher costs for picking and packing) or a dicing foil, which can be discarded after use.

Substrate

The substrate chosen for this module was FR4, a fire retardant substrate selected because of its low cost and suitability for flip chips. The critical point in flip chip design is the solder bumps, because the large difference in coefficient of thermal expansion between the die and the substrate is capable of shearing or distorting the bumps during normal temperature cycling. For this reason, the majority of flip chip designs use an underfill material. Flip chips have been successfully mounted not only on FR4, but also on flex, ceramic, and silicon substrates.

Lines and spaces of 100 µm (or even 75 µm) are usually required on flip chip substrates; therefore, the design and production of the substrate are critical stages. When flip chip I/O counts become large, laser-drilled or photo vias must be used because conventionally drilled vias lack the needed precision. The solder mask on the substrate should be as thin as possible because sufficient gap height is needed under the chip for flow of the fluid underfill material. Registration between the metal layer and the solder mask is a frequent production problem; mechanical registration, for example, yields a typical accuracy of ±50 µm, which is inadequate for most applications.

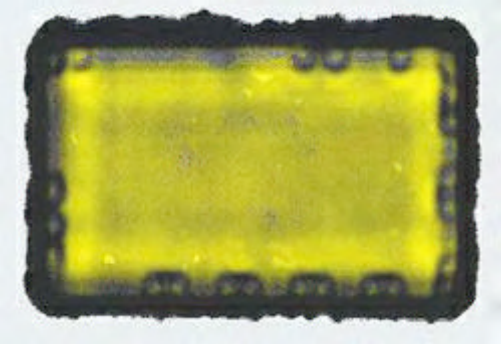


Figure 2. Acoustic image of defect-free flip chip. The yellow area is the underfill. Careful material selection and process design avoided internal defects such as delaminations and voids, which would stand out in high contrast in an acoustic image.

In development work for this flip chip application, panels of 63 substrates were used (see Figure 1). The FR4 substrate material had one copper (Cu) wiring layer. As part of development, four different surface finishes were applied to the copper: organic solderability preservative (OSP), nickel gold (NiAu), chemically plated silicon (Si), and silver (Ag). After assembly, electrical measurements showed differences in yield among the four surface finishes. Although the differences identified among the surface finishes were

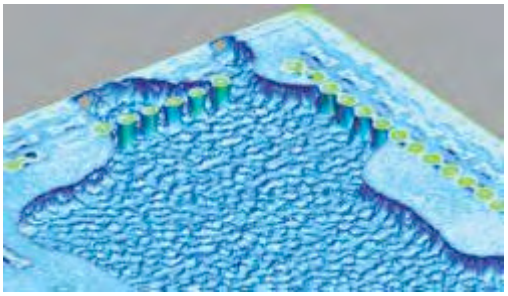
considered proprietary, the process enabled the institute to select the one most appropriate for the application.

The size of the lands on the substrate should be the same size as the bond pads on the flip chip itself, typically 80–100 µm. The goal of chip placement is to ensure that the solder bumps are at least in contact with the edge of the lands in order for the bumps to self-center during reflow. If the lands are correctly placed on the substrate, the maximum placement tolerance for the flip chip is 40–50 µm. If the location of the lands is imperfect, the tolerance needed to ensure that the bumps are in contact with the edges of the lands will be lower.

Fluxing, Placement, and Soldering

For placement, vision systems typically recognize SMD components by their shape, but these systems do not work well with flip chips because size varies with the accuracy of the dicing saw. Flip chips are usually recognized by the bump pattern, requiring a technique that uses a high-resolution camera. Because the bumps are on the face of the die, the camera can mistake some nonbump features, such as large metal structures, for bumps. To compensate, an engineer may choose to program the vision system to exclude specific bumps from the recognition pattern.

Figure 3. Acoustic image of a flip chip(not from this application) showing a large void area where underfill material is absent.



Flip chips need more flux than conventional SMDs for tacking the flip chip to the board and for solder activation during reflow. Two methods are used for applying the flux. The flux can be dispensed or sprayed onto the board, which requires a flux that will leave minimal residue after reflow. Alternatively, flux can be deposited onto the chip bumps by dipping the chip into flux. In this case, flux viscosity must be higher to ensure that the flux adheres to the bumps, and flux application must be carried out in the placement machine just before placement.

It is extremely important to avoid flux residue in flip chip packages, because the tightness of the gap makes cleaning processes impractical during production. Flux residue is a frequent cause of nonwetting and poor adhesion during underfilling. For example, flux residue on a solder bump can result in a void adjacent to the bump postcure. Solder will eventually creep into this void. When the flux is dispensed or sprayed onto the board, it is important to ensure that the flux and the underfill material are compatible.

For this application, the flux dipping process was used. Because previous studies have shown that the soldering yield is higher if soldering is performed in an inert atmosphere, reflow soldering was carried out in a nitrogen atmosphere.

Key Points of the Flip Chip Package

Flip chips are so named because the silicon die (the "chip") is mounted with the active side down on the substrate. More-conventional packages—such as plastic quad flat packs, small outline integrated circuits, and dual in-line packages—have the active side of the die upward and are connected to the substrate by bond wires running from bond pads on the top of the chip down to the substrate.

A flip chip is connected directly to the substrate by small solder bumps. During manufacture, the solder bumps are attached to the die face (or sometimes to the substrate) before the die is positioned face down on the substrate. During the heat of reflow, the solder bumps complete the electrical connections from the active circuitry of the die to the substrate. On the die face, the solder bumps may be arranged peripherally or across the area of the die.

Because there is a significant difference in the coefficient of thermal expansion between the die face and the substrate, the space between the die face and the substrate is almost always underfilled with an epoxy material. The epoxy is dispensed at one or more sides of the gap beneath the flip chip and flows by capillary

action until it fills the space and makes contact with all of the solder bumps. The effect of the cured underfill material is to reduce strain on the solder bumps by a factor of about 10.

Flip chips have several advantages over other electronic package designs. The shorter distance from the active circuitry of the die to the substrate means faster conduction, which can translate into improved performance. Flip chips can also save space because no space is required for bond wires and because the silicon itself can be made thinner. In a conventional DIP, for example, the silicon of the die is usually about 640 µm (0.026 in.) thick. Flip chips have recently been developed in which the silicon is only 50 µm (0.002 in.) thick.

When mounted on a PC board, flip chips look unlike other IC packages because the silicon die is not encapsulated in black epoxy. Because the underfill material between the die face and substrate protects the interconnects from moisture and contamination, overmolding the back of the flip chip with epoxy is unnecessary. What one often sees is the bare silicon of the back of the die. Designers can take advantage of the exposed silicon for heat dissipation by adding a metal heat sink to it. The heat sink is usually larger in area than the die itself and is usually attached to the back of the die by a thin layer of adhesive.

Overall, the flip chip package achieves simplicity, high conduction speed, and a low profile, but demands careful design and tight control over production processes. Design of the dispensing process for the fluid underfill material must avoid trapping bubbles that become voids in the cured underfill. Dispensing must also be performed in a time frame short enough to match production needs. Flux residue and other contaminants can prevent the fluid underfill from wetting the solder balls, the substrate, or the die face.

The technology necessary to solve flip chip design and production problems now exists. In a recent study designed to test the practical limits of the flip chip design, researchers at the Fraunhöfer Institute (Berlin) successfully mounted and underfilled flip chips for which the silicon die measured 40 x 40 mm x 1.57 in.). During underfill, the fluid epoxy achieved complete contact with each of the 5770 solder bumps.

Because of their high speed and low profile, flip chips are often used in small systems where space is at a premium. Handheld devices, for example, use many flip chips. Despite their sophistication, development has now reached the point where the implementation of a flip chip design often costs no more than the implementation of larger, more-conventional electronic packages.

Underfill

Selection of the underfill material and dispensing method are critical steps in designing flip chip assembly. The cured underfill serves multiple functions. It compensates for the difference in coefficient of thermal expansion between the substrate and the chip. It also protects the solder bumps from environmental contaminants (see Figure 2). Some of the defects that can originate during flow of the fluid underfill are delaminations (where the underfill fails to wet and adhere to a surface) and voids (where contamination causes local variation in the speed of flow and causes bubbles to be trapped; see Figure 3). Proper material selection and dispensing can increase the life of a flip chip package from a few to more than 4000 thermal cycles. Because the failure of a single flip chip—or any other device—will at least impair and probably kill an entire system, the reliability for thousands of cycles is important. This is why most warranties are relatively short term: of the failures likely to happen, most will happen early.

The cost of underfilling is also a consideration. Manufacturing costs of a chip are lower when the flow time and cure time are both minimized. Flow time and avoiding defects such as voids are in part determined by the dispensing pattern.

Although the fluid underfill is frequently dispensed along one or two sides of the chip, the best results in this application were obtained by dispensing a large dot of fluid underfill material with a wide needle at one corner of the chip.

Figure 4. Fraunhöfer IZM's assembly line.

Three underfill materials were selected and evaluated with this process. The most successful, which was selected for production, had no filler particles, flowed rapidly, and had a cure time of 3 minutes at 150°C.

Analysis of Sample Packages

A critical part of the development process was the analysis of sample packages. The two key analytical tools were x-ray and acoustic microimaging. A FeinFocus (Stamford, CT) x-ray system with a resolution of 10 µm was used to image features such as improper solder volumes and misalignments.

Acoustic microimaging uses very-high-frequency ultrasound. A Sonoscan C-SAM system (Elk Grove Village, IL) was used, which pulses ultrasound into the flip chip package and receives the return echoes. Although x-ray is sensitive to changes in the bulk of a material, acoustic microimaging is sensitive to both internal bonding and lack of bonding.

Flip chip packages are ideally suited for acoustic microimaging because the silicon die is transparent to ultrasound. Ultrasound pulsed through the die, therefore, produces sharp acoustic images of the solder bumps and underfill material. Well-bonded interfaces, such as the bond of a solder bump to the die face, are imaged in normal contrast, whereas gap-type defects such as voids or delaminations are imaged in the highest contrast.

For this application, the ultrasound was used both for characterization of underfill materials and for imaging of the underfill-solder bump layer in the finished chip packages.

Characterizing underfill materials before prototyping was one of the key elements in the success of this application. The completed prototypes experienced no failures when put through the OEM's standard tests.

Conclusion

Careful selection of processing method and materials resulted in the successful development of production steps for this flip chip to speed development of the final product (see Figure 4). Medical electronics manufacturers can use this advanced technology without incurring increased production costs. Flip chips are smaller—which usually means both a smaller area and a lower profile—than conventional electronic packages, and they offer faster conduction speed. Most critical was the investigation of the flow pattern, flow time, and cure time for three underfill materials and the selection of those materials for production. During development, 1000 prototype devices were assembled by an SMD and flip chip assembly line. Two devices failed because of incorrect placement, but subsequent reliability tests at the OEM's facility revealed no defects. The cost for high-volume production is no more than the cost of using an SMD component for the same application.

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Back to the Fall 2000 Table of Contents