Preventing flip-chip solder joint failures

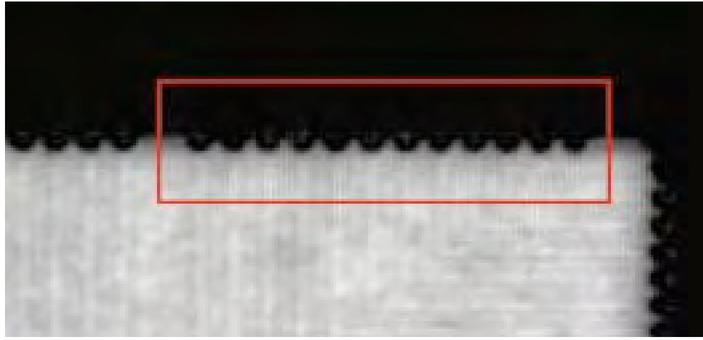

Figure 1: Acoustic image of one corner of a test chip before thermal cycling. Solder joint bonds are dark and it merges into the background since there are no fractures.

Delaminations between the chip face and the cured underfill are widely thought to be one of the most prevalent causes of electrical failure in flip-chip on board (FCOB) packages. The failure mechanism is usually described as severing of a solder bump interconnect by the expansion of a delamination.

But the data–both formal and informal–concerning this type of failure is not consistent. In some FCOBs, solder bumps become disbonded or cracked without the presence of a delamination. In others, a delamination may surround one or more solder bumps and cause no immediate damage. Fractures in solder joints have even been observed that resulted in no immediate loss of electrical function.

In order to shed more light on the degradation of solder joints in FCOBs, a joint research project was undertaken between DaimlerChrysler SIM Technology and DaimlerChrysler Research Institute. The focus of the study was on the degradation of solder joints over time as a result of thermal cycling. Thermal cycling exaggerates the already large difference in the coefficient of thermal expansion between the substrate and the silicon die. Strains caused by thermal cycling are most severe at the corners of the die. The study also sought answers to specific questions: How are solder joint cracks initiated? How do these cracks propagate? What is the role of micro-structural coarsening of the solder joint?

The test chips measured 6.3mm-by-5.6mm and had 96 peripheral eutectic SnPb solder bumps with a pitch of 20μm. Alternate bond pads were connected to create a daisy chain structure. An infrared reflow process was used having a peak temperature of 230°C. Fluid underfill was dispensed along one side of the chip and flow was completed in about 20s at 60°C to 70°C. The substrate was an FR4 printed wiring board having Cu pads with a Ni/Au overlay. A portion of the test chips–manufactured by Flip Chip Technology Co. Ltd–were left without underfill in order to determine the average time-to-failure when the solder joints had no protection from stress.

The test chips were subjected to thermal cycling with temperature extremes of -55°C and 125°C. Dwell time at each temperature was 30 minutes and changeover time was <10s. The chips were tested for electrical continuity and for electrical resistance of solder joints approximately every 200 cycles. They were also imaged acoustically by a Sonoscan's acoustic microscope. Selected chips were cross-sectioned and the solder joints examined with a metallographic microscope.

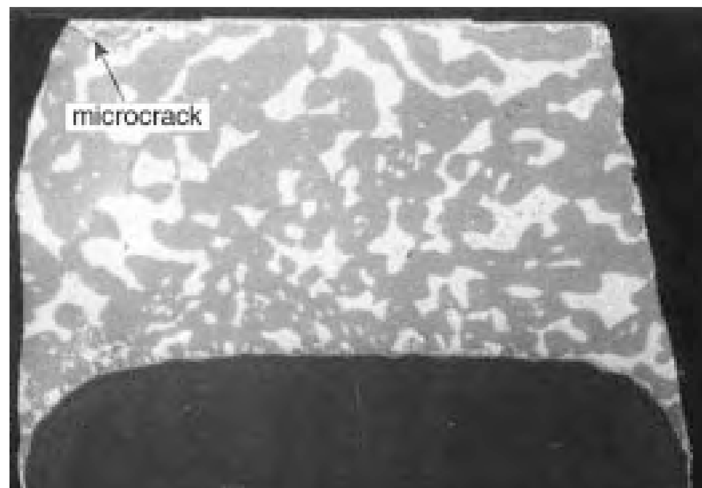

Figure 3: Crack initiation visible in a cross-sectioned solder joint where acoustic imaging had indicated crack formation.

Those chips lacking underfill failed electrically after an average of about 100 thermal cycles, while underfilled chips typically failed after more than 2,000 cycles. The role of the underfill material in redistributing the thermal cycling stresses increased the lifetime of the flip-chip packages by a factor >20.

Acoustic imaging

Acoustic imaging of the underfilled flip-chips was performed in order to achieve a qualitative assessment of the solder joints between the die face and the solder bump non-destructively. Cracks in solder joints, like any other gap-type defect, reflect virtually all of the ultrasound back to the transducer. Therefore, the return echoes from cracked solder joints have higher ultrasonic intensity than the echoes from intact solder joints and also have higher contrast in the acoustic image. As a crack propagates across a solder joint, the acoustic image of the joint becomes progressively brighter. The use of acoustic micro-imaging made it possible to determine non-destructively which solder joints were beginning to crack and served as a guide for selecting samples for destructive analysis.

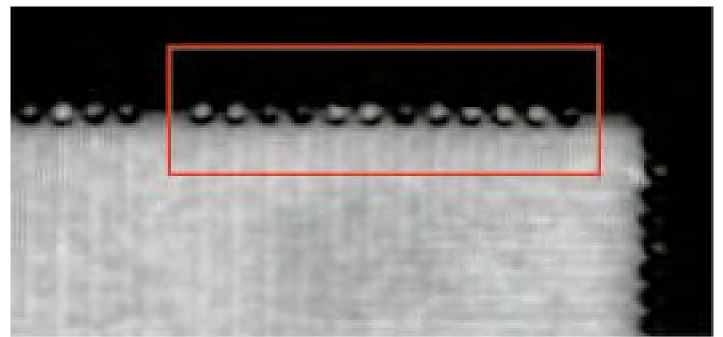

Figure 2: Test chip imaged acoustically after 772 thermal cycles. The solder joints show varying degrees of brightness, corresponding to the percentage of the bond area that has cracked.

Test criteria

Test chips matching three criteria were selected for physical cross-sectioning:

- Chips that were electrically functional and in which C-SAM imaging displayed no cracks or delaminations.
- Chips that were electrically functional, but displayed a delamination in the acoustic image.
- Chips having an open or a transient open, and displaying a delamination in the acoustic image.

Only those solder joints that displayed an increase in brightness in the acoustic image were found after physical sectioning to have cracks in the solder joint. No solder joint displaying unchanged acoustic contrast was found to be cracked.

All of the solder bump bonds are dark, indicating low contrast and therefore good bonding. After 772 thermal cycles, several solder bumps in the acoustic image of the test chip have become much brighter. These bumps display varying degrees of brightness that correspond to the area of the crack

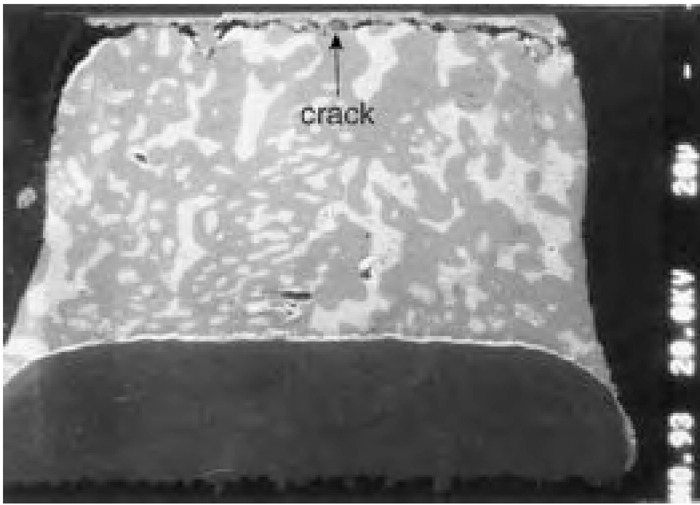

Figure 4: Complete cracking of a solder joint across the region of greatest coarsening of the solder.

in each bump.

Significantly, these cracks are forming in the absence of a delamination, which would be visible acoustically because, like a crack, a delamination represents a gap-type feature that would reflect nearly all of the ultrasound. To learn more about the formation of the cracks, some of the test chips that displayed cracks acoustically were physically sectioned, then examined and photographed with a metallographic microscope.

For a solder joint in which crack initiation has just begun, you can find some coarsening effects on the microstructure. This coarsening is more pronounced near the interface between the solder joint and the die face at the top of the photo. Finite element simulations in previous studies have shown that coarsening of the microstructure induces strains in the solder. Both coarsening and strain are most prevalent in the area of the bump nearest to the chip face.

Since coarsening of the microstructure may continue with additional thermal cycling, the result of additional cycling may not be just a larger crack, but faster propagation of the crack across the solder bump.

Throughout the study, crack initiation tended to occur before delamination of the underfill material from the die face. The dominant failure mechanism in the solder joints was cracking related to microstructural coarsening, rather than fracture caused by a delamination. But it seems reasonable to assume that early delamination that comes in contact with an intact solder joint could indeed cause fracture of the joint. A delamination may be caused by thermal expansion stresses, which are greater at the corners of the die or by a loss of adhesion between the die face and the underfill.

The variable influence of delaminations on electrical continuity was also shown by solder joints that had experienced complete cracking but had not failed electrically. The electrical status of solder joints could be determined because electrical resistance measurements were made continuously during thermal cycling. It appears that the compressive force of the cured underfill is sufficient to maintain electrical continuity for a period after cracking. After additional cycles, and perhaps because of the expansion of a delamination, this force diminishes and the joint fails.

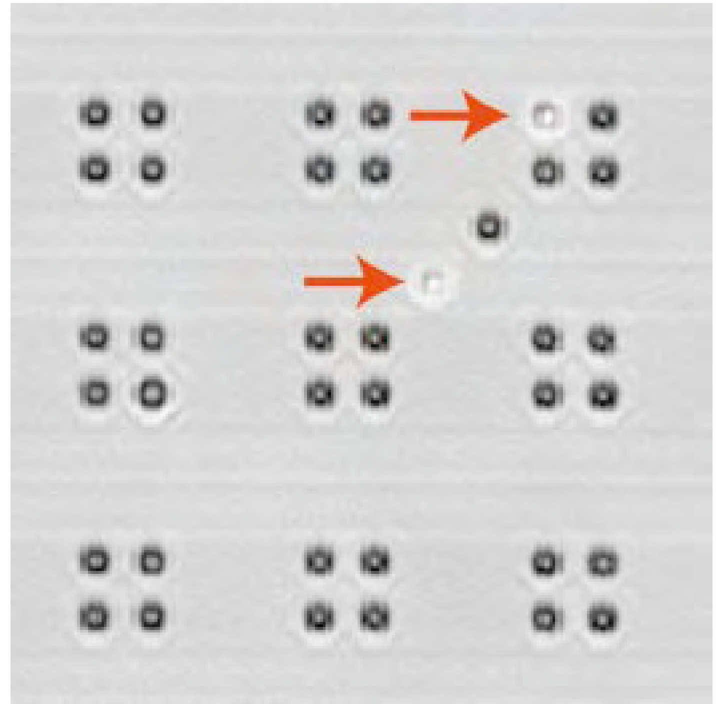

Figure 5: Ultrasonic reflectivity of solder joints at the interface to the die.

Conclusions from testing

In this group of FCOBs, where the adhesion between the chip face and the underfill was quite high, the dominant mode of solder joint failure was cracking due to microstructural coarsening of the eutectic solder, rather than cracking due to delamination of the underfill material from the chip face. During thermal cycling, failures caused by solder coarsening occurred significantly earlier than failures caused by delaminations and interaction between the solder and the underfill is understandably complex. Observations were made of solder joints where complete fracture had occurred without immediate loss of electrical function. Attention to factors relating to solder joint failure may also be helpful in achieving overall reliability of FCOBs.

[High-Density Interconnect]

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