



# Diagnosing and Avoiding Flip Chip Packaging Defects

*by Tom Adams, Consultant to [Sonoscan](#)*

Many internal defects in flip chip packages become evident only after they have affected an interconnect. The problem for engineers developing flip chip production processes is the very large number of potential internal defects that can result in interconnect damage.

Some defects cause immediate electrical failure. Other defects initiate more gradual damage that may result in a field failure even though the component and the board successfully passed electrical and functional tests. For example, a solder ball that is cracked may test good but fail in service.

The same is true of a solder ball adjacent to a void in the underfill material. The solder gradually will creep into the void at operating temperatures until the ball is deformed and disbonded. Successful process development avoids both immediate and latent failures. Some failures have their root cause during solder-ball fabrication. Individual solder balls can contain voids that may cause defects after reflow.

Balls also may vary in size from the specified diameter. A ball whose diameter is above or below the acceptable range may be identified by vision systems after ball attach. If left in place and passed through reflow, undersized balls may be attached only to the die and not to the substrate, creating an open. The excess solder in oversized balls could bridge with adjacent balls during reflow, causing a short.

Visual inspection of internal flip chip features is impossible after reflow, but the transparency of the silicon die to very high-frequency ultrasound makes internal features visible to acoustic microimaging. Each material in a flip chip package has its own density and its own velocity of ultrasound. The product of these two values is the material's acoustic impedance, and every internal interface in the flip

chip package is the boundary between two materials having different acoustic impedances.

When pulsed ultrasound meets such a boundary, a portion of the ultrasound is reflected back to the transducer as imaging data. All internal flip chip interfaces reflect ultrasound and are visible in an acoustic image. But by far, the highest contrast occurs when one of the materials is a gap such as a void, a delamination, or a crack.

If the manufacture of a solder ball created a void within the solder, the void will reflect ultrasound and be visible in an acoustic image of the flip chip package as a high-contrast gap. If the ball is intact but disbonded from the bond pad on the face of the chip, the disbond also is visible as a gap, but at a slightly different depth within the package.

In acoustic microimaging, ultrasound usually is gated by excluding all echoes except those from the depth of interest. Gating can be on the bond to the pad, on the bulk of the solder ball, or at some other depth. For example, precise gating can distinguish a bond pad disbond from a horizontal crack in the chip's passivation layer just above the pad (see Figure 1 in the May 2001 issue of *Evaluation Engineering*).

Most flip chip packaging defects have their root cause not in ball integrity or ball placement, but in the underfill process. The fluid epoxy underfill may contain up to 70% filler particles.

An important packaging design step is balancing particle size and quantity with the viscosity, cure rate, and other properties of the fluid epoxy. The fluid underfill is dispensed along one or more sides of the flip chip and flows by capillary action into the gap between the die and the substrate.

Successful dispensing means that the fluid underfill makes intimate contact with the die face, the substrate, and the sides of all solder balls. The underfill should contain no voids (bubbles). A key element in designing the dispensing pattern is the avoidance of flow wavefronts that converge in such a way to trap air bubbles.

Some of the more frequent internal defects that occur during the underfill operation and that are visible acoustically postcure include the following:

- Delamination of the cured underfill material from the die face. A delamination at this interface is serious even if it does not cause an immediate electrical failure. It is the nature of delaminations to grow with repeated thermal cycling, and

even a small delamination has the potential to expand until it encounters and breaks a solder bump.

Some manufacturers regularly use acoustic imaging to scan production for this defect. The correlation to failed solder bumps is not absolute: solder bumps sometimes crack for other reasons, and a delamination occasionally will travel around a solder bump without immediate electrical consequences.

But even in this case, the delamination provides an empty space that the solder eventually will flow into. Delaminations at this interface also create a thermal barrier that impedes heat flow from the die face.

Die-face delaminations have two chief causes: contamination on the face of the die, or a material property mismatch between the flow properties of the fluid underfill and the surface tension of the die face.

- Significant underdie areas that lack underfill material. Acoustically, these areas are somewhat like voids, but larger. They result from improper calculation of the dispensing volume. Delaminations (generally thin), no-underfill areas (generally thick), and voids (of varying thicknesses) all reflect ultrasound in high intensity, even if the thickness of the gap is as little as 100 Å. It is not unusual for the die to crack above any but the smallest voids or unfilled areas.
- Voids related to the underfill dispensing pattern. The fluid underfill is sometimes dispensed along two sides of the die. The converging wavefronts can trap bubbles that become voids. The voids often are distributed along a diagonal axis where the wavefronts met.
- Voids related to filler particle size, viscosity, and solder bumps. During capillary flow, a wavefront will slow down when it encounters a solder bump (See Figure 2 in the May 2001 issue of *Evaluation Engineering*). Wavefront speed also drops with distance traveled. The flowing underfill may fail to meet on the far side of a solder bump, resulting in a trailing void. Speed also drops if the diameter of the filler particles is more than one-sixth of the gap height between the substrate and the die face and is decreased if the fluid underfill is too viscous. High viscosity, often controllable by changing the substrate temperature, causes each filler particle to be surrounded by a sticky layer of epoxy that effectively increases the particle's diameter. As a result, the particles are more likely to collide and stick together.
- Voids related to substrate topography. Irregularities such as vias in the substrate can change the local direction of flow by 90°. As a result, speed is decreased. The formation of voids over vias and other substrate irregularities occurs frequently.

Redesign of the substrate to avoid abrupt changes is sometimes required.

- Voids related to flux residue on solder balls. Flux residue on the sides of solder balls may prevent the fluid underfill from making intimate contact. The result is a vertically oriented, usually rather narrow void encompassing most or all of the circumference of the solder ball. Acoustically, these voids look like rings around the balls and are called halo defects.
- Voids related to filler particle agglomeration (See Figure 3 in the May 2001 issue of *Evaluation Engineering*). Various factors, including the sticky layer, may cause filler particles to be distributed unevenly in the underfill. Some regions have high concentrations of filler particles and therefore relatively less epoxy while other regions have few particles. Voids are very likely to form in areas of high particle concentration. Particle distribution itself is visible acoustically because of reflections from the interface between the particle and the epoxy. Uneven distribution may occur in the X-Y dimensions, or the particles may settle out onto the substrate to create a two-layered underfill. Settling often is related to low viscosity. In some cases, both uneven horizontal distribution and settling occur.
- Irregular filler particle distribution without voids (See Figure 4 in the May 2001 issue of *Evaluation Engineering*). Even without the presence of voids, irregular distribution of filler particles can create localized thermal stresses that are harmful to the long-term reliability of the package. The risk this phenomenon poses to reliability has only recently become apparent.

External heat sinks, although not strictly part of the flip chip package, also can cause device failure. Heat sinks, usually copper, generally are adhesively bonded to the back side of the silicon die. The effectiveness of the heat-sink function is strongly dependent on applying a layer of adhesive whose thickness is within narrow limits across the whole area of the die.

Variations in adhesive thickness can restrict heat transfer and cause the die circuitry to overheat. A new technique uses acoustic microimaging to accurately measure the thickness of the buried adhesive.

### **About the Author**

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