

CSP and micro-BGA Process and Damage Assessment with Acoustic Micro Imaging (AMI)

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ABSTRACT

With the push towards lead-free solders, due to the environmental concerns about lead, there are other concerns and disadvantages that need to be addressed. One concern is the higher temperatures needed to reflow the solder. Unfortunately, the components also are subjected to these higher temperatures. The smaller types of components, such as CSPs and micro-BGAs, experience the largest delta temperature change during the reflow process. The potential for these components to see a temperature as high as 255°C in a short period of time is a reality.¹ Therefore it becomes necessary to evaluate these components for unacceptable physical damage on a pre and post reflow process basis.

One of the ways to assess the damage is via a non-destructive technique called Acoustic Micro Imaging (AMI). AMI can be used to characterize any physical defects that may pre-exist in the CSP, etc., due to manufacturing and allows you to evaluate the same sample after reflow for any additional damage. Example data is provided for the categories of defects to be concerned about during manufacturing and after the reflow process. Emphasis will be placed on the “critical” defects for CSP and micro-BGA type packages.

INTRODUCTION

Acoustic Micro Imaging (AMI)

There are several commercially available AMI based systems, ranging from basic laboratory type models to fully automated systems for analyzing larger volumes of parts on an automated basis.

All reflection mode based AMI systems start off with one basic piece of AMI information called the A-Scan. The A-Scan is obtained by sending a pulse of acoustic energy from a transducer and into the sample under investigation at a specific X-Y location and then looking for the return of any echoes, see Figure 1. Depending upon the construction of the sample/part, there can be multiple echoes or a single echo from the backside, assuming a solid, defect free material. The returned echoes make up the A-Scan and are typically displayed on an oscilloscope.

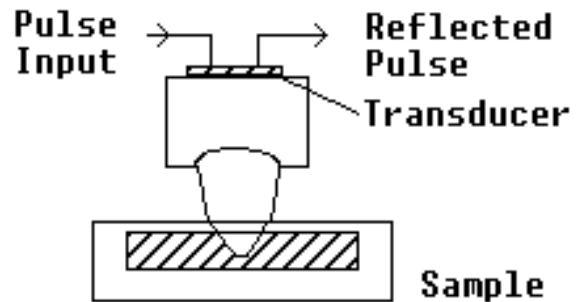


Figure 1. Block Diagram Of The Transducer Section Of A Reflection Mode AMI System.

The echoes can be interpreted, since any interface between two materials within the part will cause some of the acoustic energy (echo) to reflect back to the transducer. The amount (amplitude) and form (polarity) of the returned energy is dependent upon the differences between the acoustic properties of the materials, in particular the acoustic impedance (Z) mismatch.

Acoustic impedance (Z) is a physical property based on the velocity of sound and density of the material. When two materials are bonded together, the amount (amplitude) of energy reflected is based on the difference between the two materials' acoustic impedances. A large difference will cause most of the energy to be reflected back to the transducer and a small difference will allow most of the energy to be transmitted to the next material. This data is obtained from the amplitude of the A-Scan at that interface. The polarity of the A-Scan tells additional information.

If the polarity is positive, we know that the first material has a lower acoustic impedance than the second material. If the polarity is negative, we know the first material has a higher acoustic impedance than the second. A simple example would be two silicon wafers bonded together, see Figure 2.

Two properly bonded silicon wafers would not have any reflection from the interface, since they are the same materials, most of the energy is transmitted to the second silicon wafer. If the first wafer is not bonded to the second, some gap exists, which could contain air or be a vacuum.

In either case, most of the energy would be reflected back and would have a negative polarity. It would be negative since silicon has a high acoustic impedance and air/vacuum is low, practically zero.

With this information collected at all X-Y locations of a part, you can image the locations of defects in the X, Y and Z directions within the part. The most common image type is called a C-Mode, an X-Y plane at a particular depth Z within the part. Further processing of the data can provide non-destructive cross sectional information and other forms of images/data for evaluation.

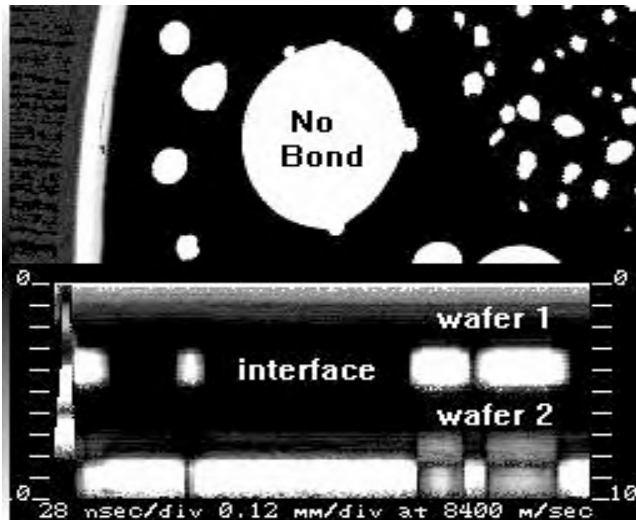


Figure 2. C-Mode Image (Top portion) And Non-destructive Cross Section Called Q-BAM™ (Bottom Portion) Of Two Wafers With Bonded And Non-Bonded Areas.

Lead Free Solder Initiative

There has been pressure for a number of years by environmental groups to get the lead out of solder. Within the last few years these pressures have increased with the “Green” movement throughout the USA, Japan and Europe. These environmental movements have component manufacturers, solder suppliers and PCB assemblers looking at alternatives to solders containing lead.

At this point in time, all of the lead free solder alternatives require higher processing temperatures, up to 255° C. Unfortunately, the use of these higher temperatures may cause other problems with the PCB and component materials. One of the programs evaluating the new lead free solders is being headed by NEMI. The study also includes looking at the requirements for PCB materials, lead finishes, the reflow process, component damage and solder joint fatigue.²

The NEMI program is just starting (July 2000) with an anticipated completion date in early 2001. While the NEMI program will cover all of the anticipated areas of

concern, component damage is the focus of this paper. Initially the types of defects that can occur will be reviewed and then compared to observed damage, if any, upon completion of the program next year.

Surface Mounted Component Defects

At this point in time, there is no industry consensus on the types of allowable or rejectable defects at the time of device manufacture. However, individual companies and some country specific standards organizations, such as EIAJ, have their own standards of acceptance for “as manufactured” components. One of the common areas of concern is delamination on the active surface of the die near interconnections. A similar concern exists for delaminations near downbond interconnections.

However, there are universally accepted standards for defects of concern after reflow processing, due to the component’s sensitivity to moisture/reflow. These have been published as a joint IPC and JEDEC standard, J-STD-020 – Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices. While additional, similar standards cover the concerns for passive components, such as capacitors (see Figure 3), this paper focuses on the solid state devices. Based on the currently published standard, the following are defects of concern:

- External cracks visible with 40X optical microscope.
- Internal crack that intersects a bond wire, ball bond or wedge bond.
- Internal crack that extends from any lead finger to any other internal feature.
- Internal crack extending more than two-thirds the distance from any internal features to the outside of the package.
- Delamination covering the entire length of any surface-braking features.
- Delaminations showing a measurable 10% change in the following locations:³
 - On the top surface (active) of the die.
 - Any wire bonding surface.
 - Along any polymeric film bridging any metallic, isolated features.
 - Through the die region in thermally enhanced or devices that require backside electrical contact.
 - Along the polymer potting or molding compound/laminate interface for BGAs.
 - Along the solder mask/laminate resin interface for BGAs.
 - Within the laminate for BGAs.
 - Between the underfill resin and chip or underfill resin and substrate/solder mask for BGAs

The defects of concern, when observed, typically require further assessment of the devices to determine if the defects are critical for their intended usage. The assessment usually considers the environment the devices will be subjected too and the level of reliability required. One such example could be the use of the device in a child's toy versus a piece of military equipment.

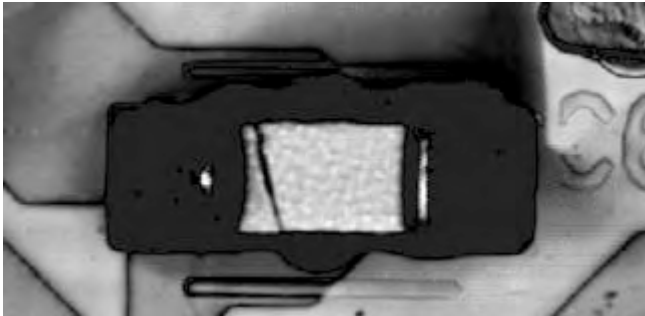


Figure 3. The Black Line Running Across The Left Portion Of The Capacitor Indicates A Crack Within It.

DEFECTS OBSERVED WITH AMI FOR SPECIFIC PACKAGE TYPES

While certain types of defects are common for many of the packaged device styles, some defects are unique to specific package designs or may appear differently due to the construction of the package. Since the focus of this paper is the newer, smaller style of packages, mainly micro-BGA and CSP types, defects observed in these types of packages will be concentrated on. However, a general review of critical defects observed in some of the more general package styles seems prudent.

General Package Defects Observed

Within the industry standard, J-STD-020, general package styles have been broken down into two general categories, "Peripherally Leaded Components" and "Ball Grid Array Packages". While both categories can experience similar defects of concern, each has its own unique weaknesses, also.

Peripherally Leaded Components

The most common defect that can be detrimental to its long or short term performance is delamination on the active surface of the die. While most general packages do have the active side of the die up, there are other designs with the active sides down.

When the parts are unmounted, it is easy to access the top surface of the die from either the top or bottom surface of the device. When the devices are mounted, it becomes a little more difficult, since you have to go through the molding compound and die to get to the active side of the chip for some packages. In these situations, its helpful to understand the construction of the parts, so you know what to expect at each interface.

One of the unique defects associated with peripherally leaded devices is the delamination between a polymeric film, such as polyimide, and either the molding compound or lead fingers, see Figure 4. The polymeric film support strip used for holding and maintaining the separation between lead fingers in not needed for BGA style packages, where the lead traces are either screened on to the substrate or integrated within the layers.

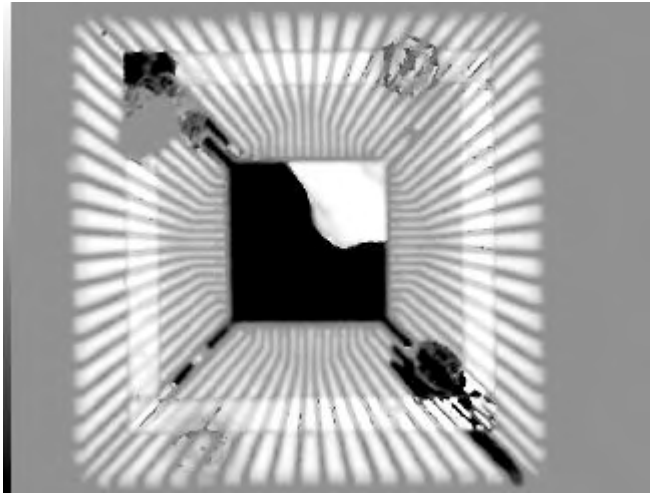


Figure 4. Peripherally Leaded Component With Delamination (Black) On The Paddle And Along The Lead Frame And Support Strip.

Ball Grid Array (BGA) Packages

In addition to the common concerns associated with peripherally leaded devices, there are unique defect types associated with the mold compound to laminate interface, with the laminate itself and the underfill, if present. The most obvious is any delamination between the mold compound and the laminate, which could lead directly to cracks within the laminate, since the weakest bond interface is the fiberglass and the resin, see Figures 5 and 6.

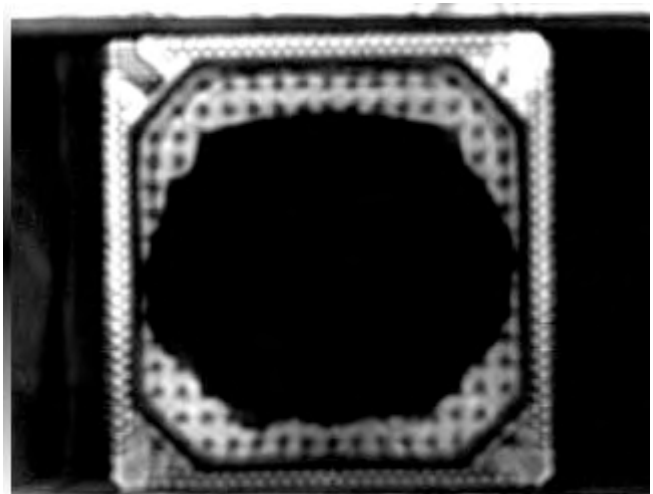


Figure 5. Popcorn Crack Within PBGA (Through Transmission Image).

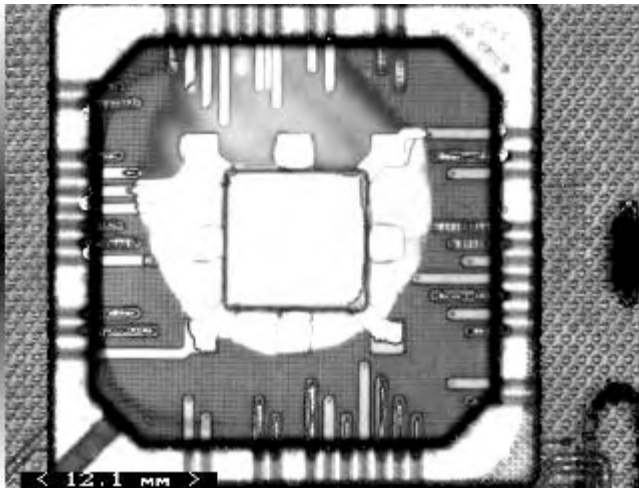


Figure 6. C-Mode Image Of Popcorn Crack Within PBGA Showing Delamination (White) Along Some Traces And Between MC And Laminate. A Crack Within The Laminate Is Observed Near The Top (Gray).

The Forgotten Defects

While not specifically covered in any of the standards, voids (large delaminations) and die cracks (see Figure 7) need to be looked at closely. Not only are they a potential reliability problem, their mere existence can be an indicator of a problem in the manufacturing process. The problem may not be significant now, but could grow out of hand over time.

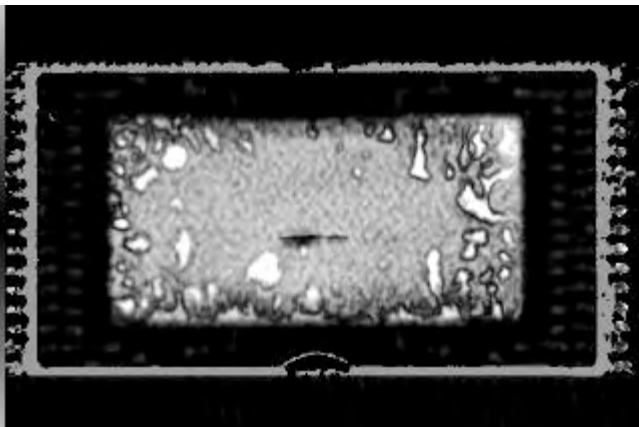


Figure 7. C-Mode Image of TSOP Device With Voids In The Die Attach (White) And Crack In The Die (Black Line Near Center).

CSP and Micro-BGA Type Package Defects Observed

New types or variations of CSP style packages seem to be developed on a daily basis. However, the types of CSP can be broken down into four basis categories, which may or may not be overmolded.⁴ The four categories are; Flex Circuit Substrate, Rigid Substrate/Micro-BGA, Lead Frame and Wafer-level/Flip Chip Based.

Each of these CSP types have their advantages and disadvantages, which need to be evaluated for the particular environmental or application use. With each type, there are unique and similar defects that need to be evaluated, also. A review of the more critical defects for each of the CSP types is provided.

Flex Circuit Substrate

The construction of the flex circuit substrate CSPs normally has solder balls attached in a matrix layout to the flex circuit. The flex circuit itself acts as the transition from the die pad layout to the matrix. Usually the die is electrically connected to the flex circuit via either wire bonds or TAB interconnections, with the active surface of the die facing up or down, see Figure 8. Normally a pliable organic material, elastomer, is utilized as a bonding and cushioning agent between the die and the flex circuit substrate. An overmold may also be applied, typically covering the die and wire interconnections and bonded to the flex circuit material.

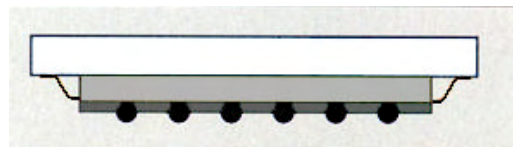


Figure 8. Diagram Of Typical Flex Circuit CSP With The Active Surface Of The Die Down And With TAB Interconnections.

Defects of concern include any direct disconnections of the circuitry, such as poor solder bump bonds, trace or via breaks in the flex circuit, poor TAB or wire bonds, wire breaks and cratering under the bond pads. Indirect defects that may cause failure on a longer term basis include, voids or cracks in the elastomer material or the mold compound, when overmolded. Due to the mounting process, environmental and/or operating conditions, these benign defects may become deadly. See Figures 9 and 10.

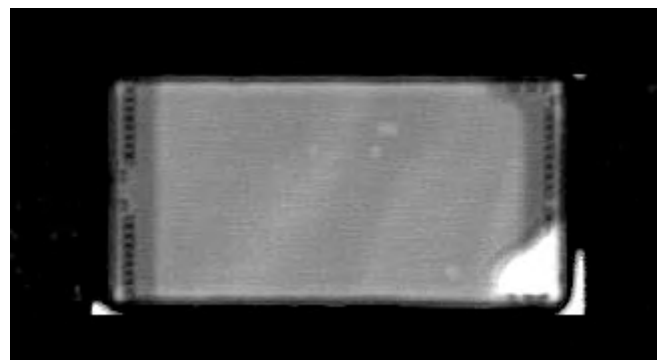


Figure 9. C-Mode Image Of Flex Circuit CSP With Delamination (White) Between the Die and The Elastomer In The Bottom Right Corner.

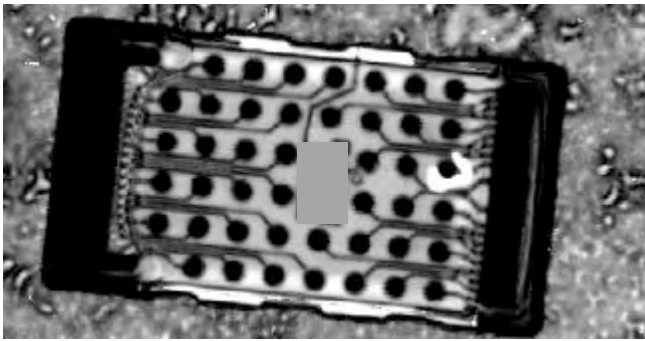


Figure 10. C-Mode Image Showing A Delamination (White) Between The Flex Circuit And The Elastomer.

Rigid Substrate/Micro-BGA

Similar in construction to its larger sibling, PBGAs, these types of packages have common weaknesses, also. The overall structure has a matrix of solder balls attached to the rigid substrate. The multiple layers of the substrate, consisting of metal traces layered between resin/glass, also redistribute the matrix pattern to a die pad pattern. The die may be electrically connected via wire bonds using a conventional die attachment, see Figure 11, or via a flip chip with underfill arrangement. Again, the die and interconnections may be over molded to provide protection to the die and interconnects.

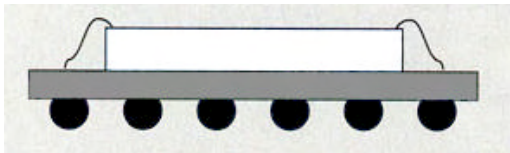


Figure 11. Diagram Of Typical Rigid Substrate CSP With Wire Bonds And Die Attach.

Similar defects of concern are present for these types of packages as for the flex circuit types. There is the addition of multi layer substrate, which due to its resin/glass construction is more vulnerable to internal defects than the flex circuit materials, in most cases, see Figures 12 and 13.

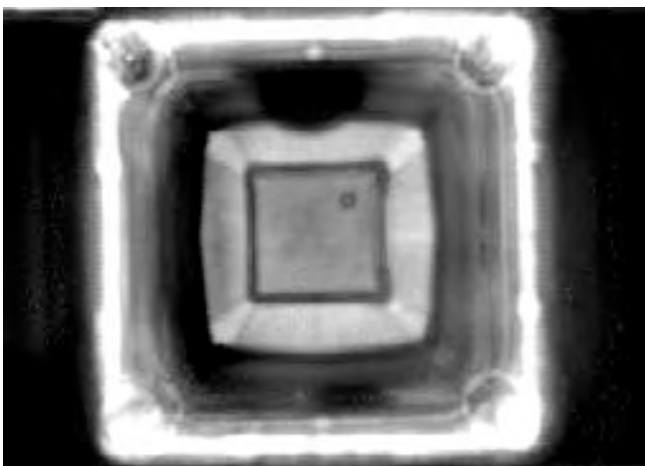


Figure 12. Micro-BGA With Delamination (Black) Within It Observed With Through Transmission.

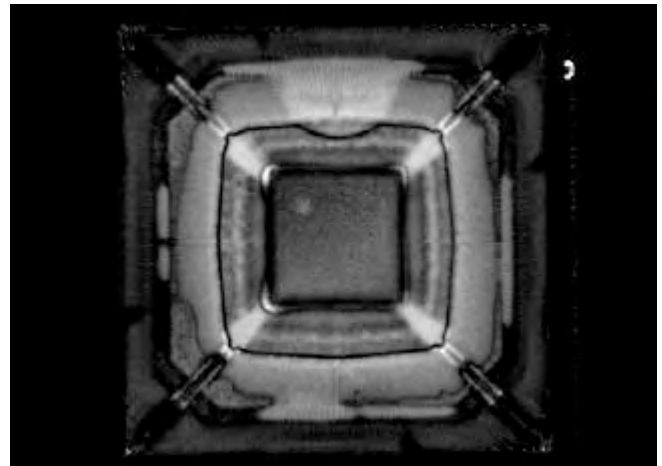


Figure 13. C-Mode Image Of Same Micro-BGA With Delamination And Small Void In The Die Attach.

Lead Frame

Also similar to its larger siblings, PEMs (Plastic Encapsulated Modules) or Peripherally Ledged Components, with the one exception that the die is generally the biggest volume of the package, in comparison to the lead frame and the molding compound present. The most common could be considered a LOC (Lead on Chip) type package, See Figure 14.

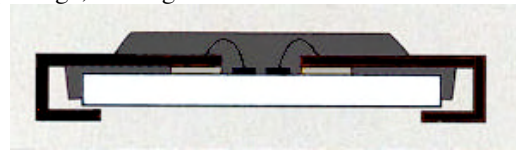


Figure 14. Diagram Of Typical Lead Frame CSP.

Again, defects considered detrimental to the larger packages should be considered more critical, since there is little material beyond the die. In addition, cracks or delaminations between the die and the lead frame should be seriously evaluated, see Figure 15.

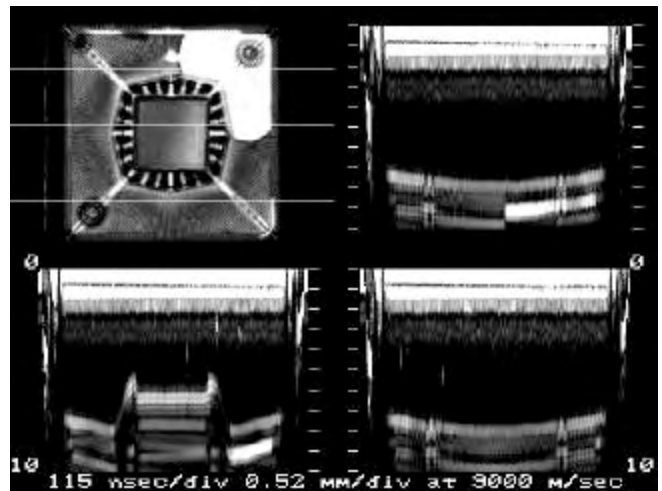


Figure 15. C-Mode (Upper Left) And Multiple Q-BAM™ Images Of Lead Frame CSP With Delamination (White).

Wafer-level/Flip Chip

Obviously there are not too many materials or structures to deal with, beyond the die and the interconnections, typically solder bumps, see Figure 16. The interconnects may also consist of various forms of solder shapes, such as columns, or gold bump/stud interconnects. The trick is getting them properly connected and uniform (see Figure 17) and then keeping them interconnected overtime, which is usually done with some sort of underfill material.



Figure 16. Diagram Of Typical Wafer-level CSP

The underfill materials may be applied pre or post interconnect. In either case, the worst indirect defects are voids touching the interconnects, see Figure 18. Without support, the interconnects have a tendency to become unreliable over time. Cracks, delaminations and voids in high stress areas, typically at the corners should also be seriously evaluated, depending on the intended use of the CSP.

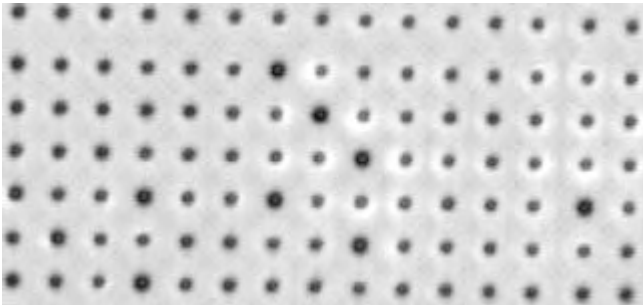


Figure 17. C-Mode Image Of A Mounted Flip Chip With Non-uniform Solder Interconnections.

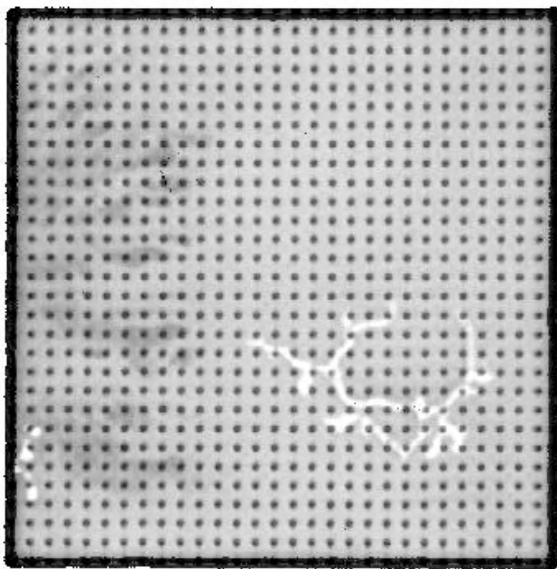


Figure 18. C-Mode Image Of Flip Chip With Voids (White) In The Underfill.

CONCLUSION AND FUTURE TESTING

At this time, the types of defects described are still considered to be “reliability” risks, which need to be discussed and agreed upon as being acceptable or rejectable for their intended usage. As more data becomes available through programs, such as the NEMI initiative for the evaluation of Lead Free Solders or released by manufactures, the criticality of the defects will become clearer.

The only unfortunate thing is that by the time all the data for a certain package type has been gathered, analyzed and categorized, it may be too late. Meaning that either the package design, materials, etc., have been modified for cost savings and/or to correct observed problems. In some cases that style of package may have even become obsolete.

Therefore, we must encourage the sharing of knowledge through standards organizations, such as NEMI, IPC and JEDEC/EIA to stop preventable failures from occurring.

Following in that direction, the package defect and damage data obtained from the NEMI Lead Free program will be available for open discussion and presented as it becomes available.

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