Chip-scale packages: Inspection methods for diverse designs

Chip-scale designs require careful control of production processes and inspection so that design specifications are adhered to. Use machine-vision inspection before packaging and acoustic imaging after packaging for better results.

By Tom Adams

A significant factor in the reliability of any chip-scale package (CSP) is the condition of the solder ball interconnects. Solder ball inspection is critical for current designs; it will become even more critical as grid pitch drops from 0.75 to 0.50 mm—a change that will probably begin next year.

One expert who has closely examined the reliability requirements of the solder ball interconnects themselves is Ed Caracappa, Semiconductor Program Manager at Acuity Imaging. "Most CSPs are high-volume flash memory. These parts will have higher production runs than conventional BGA devices," he notes.

Manufacturers of CSPs will generally find that production runs are shorter than conventional package types. The machine vision system must be sensitive to several solder ball parameters—and this sensitivity will become more important in maintaining reliability as I/O counts go up and ball sizes go down.

Examining solder balls

The first of several machine vision inspections occurs when the solder balls are placed on the fluxed pads. Your inspection at this point should cover several critical ball parameters. One parameter, missing balls and extra balls (**figure 1**), is usually the result of handling problems, which in turn is sometimes related to environmental conditions. Low humidity, for example, can cause static electricity that interferes with smooth handling. Under extreme conditions the balls may even "float" free in the air.

During the same inspection step, check the precise position of each ball. Look at the geometry of each ball. Balls are supposed to be spherical; the two most common anomalies are columnar and oval balls. "Here is where the sensitivity of the machine vision system becomes critical," Caracappa says. "Both columnar balls and oval balls can look spherical to an unsophisticated inspection system. But if these balls slip through, they cause unpredictable things to happen during reflow."

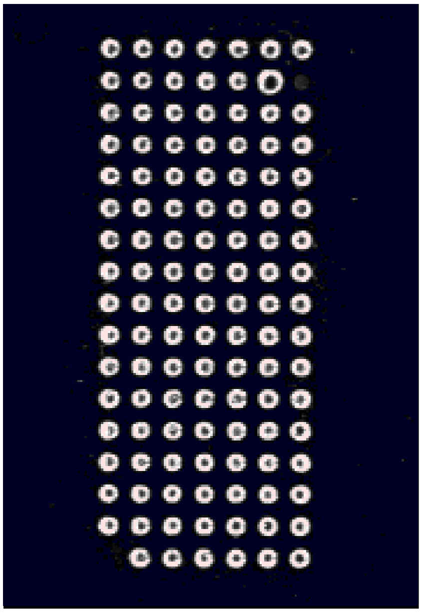

***Figure 1**: Machine-vision systems reveal both missing balls (two) and check the ball diameter (one oversized ball).*

At the same time, machine vision should look at the color of each solder ball. A chief problem is darkening the ball's surface, indicating oxidation. No one has yet determined how severely ball oxidation compromises interconnect capabilities, so darkened balls are almost universally rejected. Oxidation sets in when the balls rub against each other during handling, and can happen rather quickly.

Your machine vision should also measure the diameter of each ball. Both oversized and undersized balls (figure 1) are likely to cause defects during reflow. An undersized ball, for example, may not have sufficient vertical height to bond with the chip.

"Inspecting simultaneously for these ball parameters at the ball attach stage is the first step in ensuring reliability," says Caracappa. "Next, inspection for the same parameters is carried out after reflow, because the stresses of reflow can affect all of these parameters."

Inspect the balls again after singulation of the strips. Reason: the singulation tooling can damage a ball, move it, or knock it off. Post-singulation should also inspect for scratches on the die and the presence of foreign matter. Neither of these features is ball-related, but significant scratches and foreign matter can both cause the die to crack during testing. Even superficial scratches may, like mild ball oxidation, cause parts to be rejected on aesthetic grounds.

After testing, inspect again the ball presence/absence and ball quality. Post-test is also the point at which the small diameter—typically 10 to 12 mils—and the relative softness of the solder balls used in CSPs become an issue. Force applied to the back of the die during testing can deform the balls. If the balls merely undergo slight flattening, the deformation may be unimportant. But balls are sometimes deformed into an oval shape, and this can cause a couple of problems. First, an ovalized ball may be so short that it fails to make electrical contact. Second, the ovalized ball may be misread by a machine vision system, which measures ball diameter to gauge volume. This is where you need inspection algorithms to anticipate the problem and compensate for the non-circular ball diameter. At the same time, inspect the die for die cracks and chips at the edge of the die and for de-laminations along the edge fillet.

The final inspection—usually in two steps—occurs at the packing process. In step 1, check again for missing, damaged, or migrated balls. During step 2, inspect the device for part number markings and the orientation of pin 1.

“When a machine vision system examines the solder balls going into chip-scale packages, it must perform these very specific inspections with speed, precision, and high resolution,” Caracappa says. “It must also be quickly re-configurable in order to inspect the next line of parts having entirely different tolerances and specifications.”

Figure 3: *The acoustic image of a device reveals how the lack of underfill in certain areas causes a device to crack into several pieces.*

Acoustic micro-imaging

Acoustic micro-imaging systems are highly sensitive to internal “air-gap” type defects, which include de-laminations (**figure 2**), “disbonds”, voids, cracks, and phenomena such as variable porosity. They also image the distribution of filler particles in molding compounds and in the underfill of flip-chip assemblies (**figure 3**). But how can you use these systems with various styles of CSPs?

Post-packaging attachment and integrity of the solder bumps will be one of the main targets of acoustic micro-imaging, explains Dr. Lawrence W. Kessler, president of Sonoscan. “In this role, machine-vision systems and acoustic micro-imaging systems are complementary: machine vision locates anomalies before attachment, while acoustic systems find anomalies after packaging. The combination gives you maximum coverage for reliability, allowing rework before attachment and rejection of flawed packages after attachment,” he says.

Acoustic micro-imaging systems do not merely image solder bumps in the completed package non-destructively, they image them in specific ways, which accurately give the reliability information that manufacturers need. The overall range of ultrasound used in the systems is from 10 to 180 MHz, though newly designed transducers, specifically designed to image CSPs, go up to 250 MHz. Higher frequencies give higher resolution, and the small size of the individual solder bumps demands frequencies ≥50 MHz. When this ultrasound is beamed into the package, some of it is reflected back by different interfaces at various levels within the package. A normal bond of a solder bump to a substrate reflects enough ultrasound to image the bond—but a “disbond” at this site reflects all of the ultrasound. All other air-gap type internal defects (even those as small as voids inside individual solder bumps) likewise reflect all of the ultrasound; this is why acoustic micro-imaging systems are so sensitive to internal defects.

Figure 2: *Acoustic imaging of microSMTs at 180 MHz shows small de-laminations (red) between the silicon and epoxy layers.*

Imaging CSPs

Acoustic imaging of solder bumps in CSPs takes advantage of two advanced features. First, imaging of bond areas requires precision gating of the return echoes. In gating, only those return echoes that come from the level of interest are used; echoes returned from all other levels are ignored. Fine-gating control makes it possible to separate the bond levels at the top or bottom of the bumps.

Second, imaging solder bumps requires high spatial resolution.

The variety in chip-scale packaging

By Tom Adams

Chip-scale packages, it seems, are here to stay. The best known—with eleven licenses to date—is Tessera's µBGA, but plenty of other CSPs have been designed, and some have found their own niches. Production runs of CSPs are just beginning: Tessera's first licensed production began this summer, whereas production of the micro-SMT was started for microwave diodes in 1990 by a small company named Mpulse.

JEDEC defines a CSP as that in which the x-y area of the package exceeds the x-y area of the chip by a factor of ≤1.2. Tessera has various designs ranging from the 1.2 ratio down to 1, and ChipScale's designs cover about the same range of areas.

The emergence of these packages owes a lot to the development some years ago of ball grid arrays (BGAs). BGAs take advantage of the fact that using solder balls as interconnects saves both space and conduction time.

But solder balls also create their own problems, the most significant being that of thermal mismatch: the two surfaces of the solder ball are bonded to materials (silicon and a substrate) with very different coefficients of thermal expansion. During thermal cycling, stresses can tear loose the solder ball interconnects.

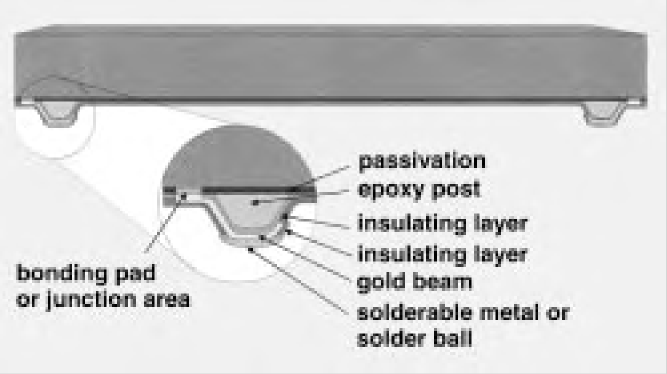

Figure: *The epoxy post and gold beam absorb the stresses created due to differences in the coefficients of thermal expansion.*

Tessera's BGA design solves the thermal expansion problem by putting an elastomer layer between the solder balls and the chip, and by connecting the chip and balls by lead bands. The chip and the substrate still undergo the same thermal expansion and contraction, but the interconnects are isolated from stresses.

ChipScale's microSMT design goes in an entirely different direction: there are no solder balls, but instead an arrangement that allows all packaging to be completed on the wafer itself. When the wafer is diced, there is no further packaging to be accomplished.

ChipScale is completing development on a completely different type of CSP called the Micro Grid Array (MGA). The active area of the flipped die has an array of compliant epoxy posts. From the bond pads on the die, a gold ribbon leads to the top of the post (**figure**). Electroless nickel with a gold flash is then deposited on top of the gold lead as the solderable metal. Why use the gold leads as an interconnect? "Gold stretches," says Jim Young, Chip-Scale president and CEO. So the epoxy posts and gold ribbon together make a compliant structure, and no underfill is needed. ChipScale intends this design, like its microSMT design, for chips with less than 100 leads.

Fortunately, the highest frequencies available (180 MHz) were developed specifically for inspection of solder bumps, and even possess an extended focal length to allow for the penetration of ultrasound to the bumps.

The result? "Acoustic micro imaging systems can non-destructively image the condition of the bonds at both surfaces of the solder bump, with the condition of the solder bump itself (oversized, undersized, absent) bridging between adjacent bumps and defects such as cracks and voids within individual solder bumps," says Dr. Kessler.

You can image from either the top side or, in some cases, from the substrate side of the CSP—a benefit in the case of Tessera's Micro BGA (**sidebar**, *The variety in chip-scale packaging*), whose elastomer layer is relatively impervious to ultrasound. ChipScale's microSMT, however, which basically consists of a silicon die, an epoxy layer, and a silicon overlay, is, in the words of one acoustic microscopist, "a piece of cake." Reason: silicon is almost completely transparent to very high-frequency ultrasound, so the epoxy layer, which is the region of high interest for internal defects, can be imaged easily and at high frequencies.