COMPONENT TEST

Achieving Long-Term Reliability in Chip Capacitors

by Tom Adams, Consultant to Sonoscan

Multilayer ceramic chip capacitors are simple in their design, which usually consists of alternating layers of dielectric and electrode layers along with terminations. Compared to active components such as integrated circuits, chip capacitors are simple indeed. But their uncomplicated design does not make them immune to problems of reliability. Nor does it lessen the impact of failure.

The failure of a single chip capacitor can have various consequences, depending on its role in a given system. A motor may fail to start; a light may be dimmed; the accuracy of a guidance system may be impaired. Chip capacitors are relatively inexpensive, but the damage that can be caused by the failure of a single capacitor can be enormous.

The basic function of a chip capacitor is to store an electrical charge. The dielectric could consist of paper, mica, or even air, but titanate and niobate ceramics generally are used because they can be formulated to yield a broad range of dielectric constants. Capacitance increases when the surface area of the electrode increases and when the thickness of the dielectric decreases.

Theoretically, a capacitor with a single dielectric layer—and consequently a huge area—would work, but it would be both too fragile and too large to use. Stacking electrodes and dielectrics in alternating layers achieves the same purpose and, by careful design of layer dimensions and chemistry, packs much greater capacitance into the area theoretically represented by a two-layer capacitor.

Multilayer ceramic chip capacitors frequently fail because the formulation of the dielectric is not within specifications. At operating temperatures, a poorly made dielectric may become conductive. The result is the formation of a leakage current.

Electrical testing focuses on identifying the capacitors that will fail in this way. Burn-in usually is performed for up to 168 hours at a temperature of 85°C or 125°C. Voltage applied during testing typically is double the rated voltage of the capacitor.

The failure rate usually is greatest during the early part of burn-in. Such electrical tests, defined by several MIL-STDs or customer needs, are very successful in identifying the capacitors that fail in service because of dielectric formulation.

Structural Defects

But electrical tests alone cannot fully qualify a lot of capacitors because failures also can occur for a second reason: internal structural defects. The important structural defects, in descending order, are voids, delaminations, and cracks. This hierarchy, which covers a large number of specific capacitor types, is based on the acoustic micro-imaging of more

than five million multilayer ceramic chip capacitors by Sonoscan's applications laboratory.

Structural defects, unlike dielectric formulation defects, do not tend to fail early in a test cycle or the lifespan of the capacitor. A void in the dielectric, for example, may serve as a route for metal migration from the electrodes even if the void is not in contact with the electrodes. Gradually enough, metal is deposited in the void to form a leakage pathway, but the time required for a failure to occur is highly unpredictable.

Many of the capacitors that arrive at the Sonoscan laboratory for imaging have already survived burn-in. Acoustic micro-imaging then can find those capacitors that have internal structural defects. The capacitors that survive both forms of testing have very high rates of long-term reliability.

Acoustic micro-imaging is most sensitive to gap-type defects which include voids, delaminations, and cracks. It detects and images delaminations and other microstructural defects even when the gap involved is less than 0.1 micron.

In acoustic micro-imaging, an ultrasonic transducer pulses very high-frequency ultrasound into the capacitor while scanning over it. The frequency of ultrasound used with capacitors usually is from 10 to 100 MHz, a range that provides good to excellent image resolution.

As the pulsed ultrasound moves downward through the capacitor, little ultrasound is reflected back to the transducer unless the ultrasound encounters a gap-type defect. A void, delamination, or crack, even of submicron thickness, reflects all of the ultrasound back to the transducer.

Since the ultrasound reflected by defects has far greater intensity than ultrasound reflected by nondefective regions of the capacitor, any voids, delaminations, or cracks are immediately obvious in the acoustic image. The usual acoustic image is a planar image, looking straight down into the capacitor, but there are other types of acoustic images.

Capacitors that have displayed internal defects acoustically sometimes are physically sectioned to expose the defect. Internal cracks generally involve several layers. Voids can exist within the dielectric, be in contact with an electrode, or involve multiple layers. Delaminations may be large or small and may exist at multiple levels within the capacitor's multilayered construction. In a planar acoustic image, such delaminations often overlap each other.

Electrically, a single delamination running along a single electrode might, in theory, be harmless. But for some high-reliability applications, it is hardly worthwhile to rely on a capacitor that has displayed any internal defect. For other applications, a small defect might be acceptable. One screening method rejects any capacitor where the diameter of a void exceeds half the thickness of the dielectric layer.

A planar acoustic image shows the X-Y dimensions of an internal defect to within 0.001 in. (25 microns) or better, depending on the acoustic frequency used. At the same time, acoustic imaging greatly speeds any physical sectioning which may be required by showing exactly where to cut.

Figure 1 is the planar acoustic image of two capacitors. The capacitor on the right has no

internal defects. The capacitor on the left has multiple large internal delaminations. In the acoustic image, these delaminations appear to overlap each other because they are at varying depths within the capacitor.

Figure 2 shows the same pair of capacitors imaged acoustically in a different way. The top half of Figure 2 presents the planar view of the capacitors but in a different color map. The bottom half of Figure 2 is a nondestructive acoustic cross section through the capacitors and shows the internal features as they would be seen in a physical cross section. The line through which the nondestructive "cut" is made is the bottom edge of the planar image at the top of Figure 2.

At the right and left of the nondestructive cross section are scale markers. The legend at the bottom indicates that each unit equals 0.35 mm. The left capacitor has four defects at depths of 2.8, 4.4, 6.1, and 6.4 units, respectively. These depths translate into 0.98, 1.54, 2.13, and 2.24 mm. Consequently, the extent and location of an internal defect can be determined in the X, Y, and Z axes nondestructively.

Figure 3 shows a group of ceramic chip capacitors imaged by a new high-throughput acoustic system. Capacitors normally are imaged singly or in small groups in failure-analysis laboratories. The high-throughput system handles capacitors in flat trays and images several thousand capacitors per hour by scanning the entire tray as though it were a single large specimen.

Image resolution is the same as in laboratory systems, and the method is extremely useful for identifying and removing capacitors having any internal defect. In Figure 3, white areas represent internal delaminations, voids, and cracks.

Summary

Ceramic chip capacitors usually fail either because of poor formulation of the dielectric or because of internal microstructural defects. Burn-in is highly successful in identifying the capacitors with poor dielectric formulations that tend to result in early failures. Microstructural defects such as delaminations, voids, and cracks are highly unpredictable in their time-to-failure but easily imaged and characterized by acoustic micro-imaging.

About the Author

Tom Adams is a writer and consultant based on Lawrenceville, NJ. He has written extensively on semiconductor topics.

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